Read Write Analyzer 2550++
Analog Channel 971++

USER'S MANUAL

Version 1.0

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CHAPTER 1

ABOUT THIS GUIDE

1.1 Scope of the Guide

This hardware user's guide covers the Read Write Analyzer (RWA) model 2550++ and the Analog Channel (ANA) model 971++.

1.2 Purpose of the Guide

All information necessary to set up, configure, calibrate, and troubleshoot the RWA hardware is provided within the guide.

1.3 Audience Definition

Hardware engineers responsible for the assembly and maintenance of a Guzik Technical Enterprises test system, including the set-up of the RWA. Knowledge of hard disk test environments is a pre-requisite for understanding the information presented in this guide.

1.4 Reference Material

References are provided to other Guzik Technical Enterprises test system hardware (such as spinstands) and software documentation.

The following is a list of the guides referenced in this document.

- *Universal Preamplifier 7 and Universal Interface 7 User's Guide*
- *Spinstand S312MP/S312MP-CF Installation and Alignment Manual*
- *Spinstand 1601 Installation and Alignment Manual*
- *Spinstand 1701 Installation and Alignment Manual*
- *WITE User's Guide* (Volume I)
- *WITE External Modules* (Volume II)
- *WITE PRML/NLTS Tests User's Guide* (Volume III)
- *WITE Developer's Kit Programmer's Reference Guide* (Volume IV)

CHAPTER 2

INTRODUCTION

2.1 The Read Write Analyzer Components

An RWA consists of four components:

- a Read Write Analyzer 2550++ (the larger bottom unit shown in the picture below)
- the associated Analog Channel 971++ (the smaller unit shown on top of the RWA-2550++)
- two small boards intended to be installed on a spinstand (the Universal Preamplifier 7 and the Universal Interface 7)

Figure 1 shows the front panels of the RWA-2550++ and the ANA-971++.

Figure 1 The RWA Front Panels

Figure 2 shows the back panels of the RWA-2550++ and the ANA-971++.

Figure 2 The RWA Back Panels

2.1.1 Read Write Analyzer 2550++

A **read-write analyzer** (RWA) tests magnetic storage components (heads, head stacks and disks). All tests are suitable for both engineering and production applications:

The basic configuration of the RWA-2550++ provides some parametric measurements and some **Partial Response Maximum Likelihood** (PRML) write-read channel tests.

- all industry-standard parametric tests
- error rate tests are performed through customer-selected PRML chips (parameters of the write-read channel and the PRML chip can be optimized automatically in a few seconds to minimize error rate)

2.1.1.1 RWA-2550++ New Features

The following list provides a short review of the new features of the RWA-2550++:

- PRML chip integration with data rates up to 800 Mbits/s
- fast PRML channel optimization standard with the RWA-2550++ (previous models of RWA had the fast optimization as an option)
- 800 Mflux/s programmable pattern generator

- 550 MHz analog bandwidth
- bit precompensation with 20ps resolution

2.1.1.2 RWA-2550++ Standard Hardware Components

The following list shows the standard hardware components of a new RWA-2550++:

- the entire RWA-2550++ is a standard item: since there is no access into the inside of this component, no further description is necessary

2.1.1.3 RWA-2550++ Hardware Purchase Options

NOTE: RWA-2550++ options must be installed by Guzik Technical Enterprises Manufacturing before customer delivery.

The following list shows the optional hardware items for the RWA-2550++:

- bit shift analyzer (VFO board) 250 Mflux/s (333 Mbit/s with 1-7 code)

2.1.1.4 RWA-2550++ Standard Tests

The following list shows tests performed by the RWA-2550++ under WITE (Windows Integrated Test Environment) software (installed on a host computer):

- track average amplitude (TAA)
- TAA asymmetry
- track profile
- off-track performance
- modulation
- pulse width 50
- pulse width
- pulse width asymmetry
- pulse width stability
- overwrite
- noise amplitude (crest factor)
- signal-to-noise ratio (SNR)
- signal-to-noise ratio (SNR) with spectrum analyzer

- spectrum analyzer
- MR read bias current saturation (referred to in the software as MR saturation)
- popcorn noise
- TAA stability
- error rate stability
- frequency
- write current saturation

2.1.1.5 RWA-2550++ Optional Tests

The following list shows the optional tests (also known as Guzik external modules) performed by the RWA-2550++. These optional tests are purchasable from Guzik Technical Enterprises:

- WITE 747 off-track performance group of tests:
  - bit shift
  - bit shift error rate
  - comparator error
- WITE Guzik media analysis (GMA) group of tests
- bit-shift analysis group of tests
- disk surface scanning group of tests:
  - missing pulse detection
  - extra pulse detection
  - super pulse detection

2.1.2 Analog Channel (ANA) 971++

An analog channel provides filtering of read-back signals, parametric measurements, and spectral analysis.

2.1.2.1 ANA-971++ New Features

The following list shows the new features of the ANA-971++:

- four plug-in filter slots with bandwidth up to 400 MHz (open filter 550 MHz)
- 800 Mbits/s PRML chip integration

- 550 MHz analog bandwith
- 400 MHz bandwidth spectrum analyzer
- all parametric measurements in bandwidth up to 550 MHz

2.1.2.2 ANA-971++ Standard Components

The following list indicates the standard components delivered with a new ANA-971++:

- one power filter board
- one analog box control board
- one 400 MHz bandwidth spectrum analyzer
- one chip adapter interface board with one slot for a PRML daughter board (one integrated PRML chip per daughter board), providing the ability to switch between different PRML chips by changing the PRML daughter boards
- one PRML chip daughter board (Venom standard)
- one read channel board with peak detection and two differentiator daughter board slots, providing the ability to switch between multiple differentiators by changing the differentiator daughter boards
- two differentiator daughter boards (selected from five different types) are used for timing asymmetry measurements and bit shift analysis only, providing the ability to switch between multiple differentiators by changing the differentiator daughter boards
- one main filter matrix board with four filter daughter board slots, providing the ability to switch between multiple filters by changing the filter daughter boards
- four filter daughter boards (selected from many different types)

2.1.3 Universal Preamplifier 7 (UP-7)

The preamplifier is part of the analog front end of the Guzik test system equipment, installed on a spinstand and provide a connection between the analog channel ANA-971++ and the universal interface 7.

Figure 3 shows the Universal Preamplifier 7 board:

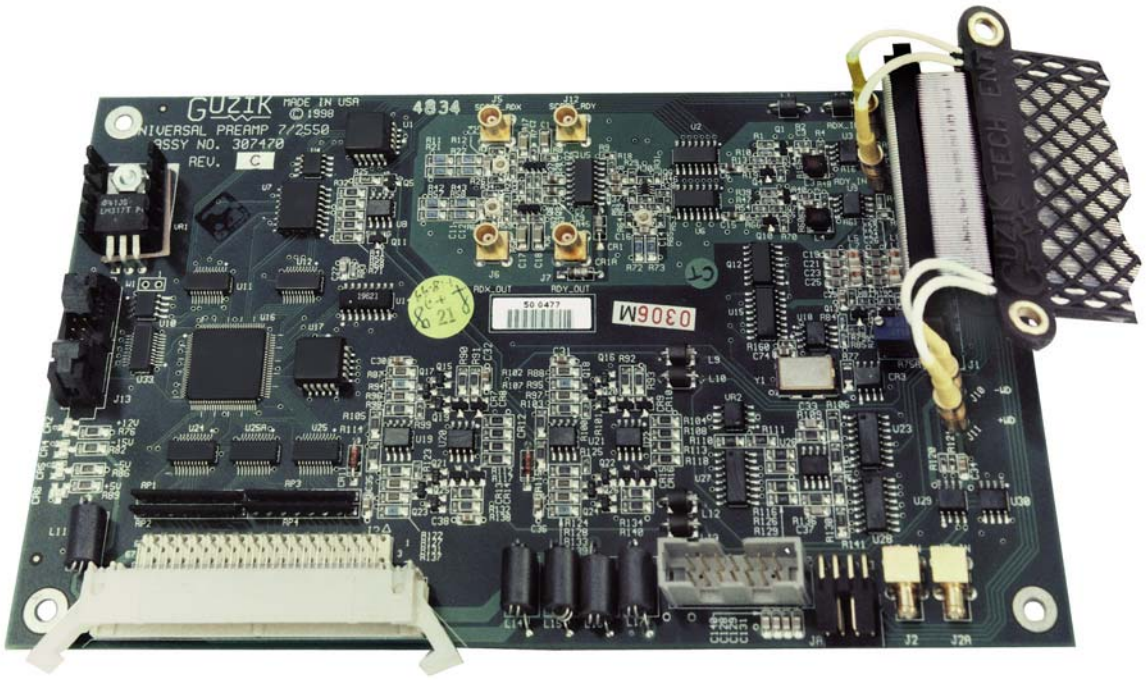


Figure 3 The Universal Preamplifier 7 (UP-7)

2.1.4 Universal Interface 7 (UI-7)

The interface is part of the analog front end of the Guzik test system equipment, installed on a spinstand between the head amplifier and the universal preamplifier 7.

Figure 4 shows the Universal Interface 7 board:

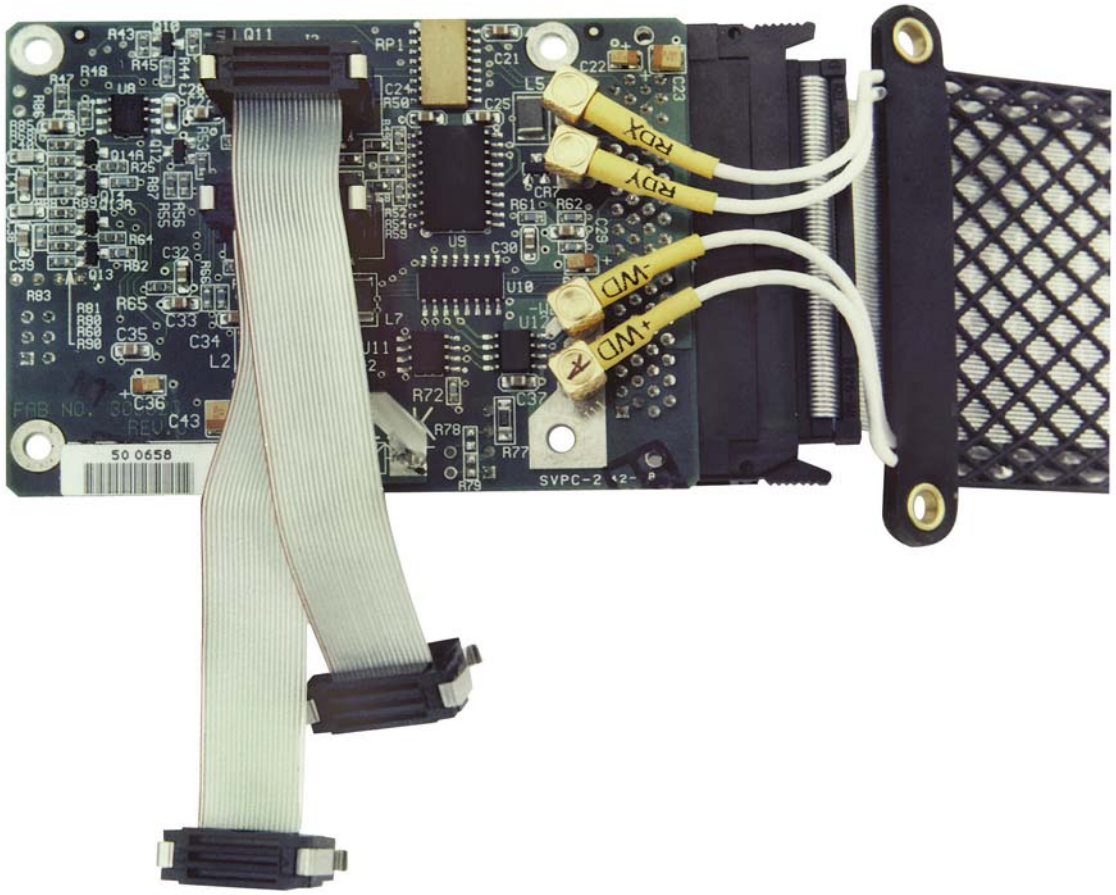


Figure 4 The Universal Interface 7 (UI-7)

2.1.5 Head Amplifiers

A head amplifier provides a connection between the head and the universal inteface 7. There are two main types of head amplifiers:

- TSA type
- Non-TSA-type

See 4.3 for details.

2.1.5.1 ANA-971++ Hardware Purchase Options

The following list shows the purchasable hardware options for a ANA-971++:

- additional differentiator daughter boards (many different types)
- additional filter daughter boards (many different types)
- additional PRML chip daughter boards (many different types)

CHAPTER 3

SPECIFICATIONS

3.1 RWA-2550++

The following specifications define important portions of the RWA-2550++.

3.1.1 Frequency Synthesizer

The following specifications define the frequency Synthesizer.

Specification Type	*Value*
Output Frequency	Up to 2 GHz with better than 1 Hz resolution
Frequency Stability	±2.5 ppm up to 75° C, ±1 ppm/year

Table 1 Frequency Synthesizer Specifications

3.1.2 Pattern Generator

The following specifications define the pattern generator.

Specification Type	*Value*
Maximum Data Rate	Up to 800 Megabits per second
Patterns	Any user-specified data pattern up to 32 K bytes of NRZ encoded data. Hierarchical pattern structure.
Precompensation	Each transition can be individually precompensated with 20 ps resolution
Jitter	Less than 3 ps RMS for periodical pattern; less than 10 ps RMS for random pattern

Table 2 Pattern Generator Specifications

3.1.3 Bit Shift Analyzer (optional)

The following specifications define the bit shift analyzer.

Specification Type	*Value*
Data Separator	5 to 250 Mflux/s (333 Mbit/s with 1-7 code)
Window Centering	100ps or 1% of window
Accuracy	100 ps or 1% window
Resolution	20 ps

Table 3 Bit Shift Analyzer Specifications

3.1.4 Accuracy of Parametric Measurements

The following specifications define the accuracy of the parametric measurements.

Specification Type	*Value*
TAA	±1.5%
Modulation	±2.0%
Resolution	±0.3 dB
SNR	±0.5 dB
Crest Factor	±2.0%
Overwrite	±0.2 dB
Asymmetry	±0.5%
Pulse Width	±1.5% or ±100 ps, whichever is greater

Table 4 Accuracy of Parametric Measurements Specifications

3.2 ANA-971++ Specifications

The following specifications define important portions of the ANA-971++.

3.2.1 ANA-971++ General Specifications

The following specifications define the general specifications of the ANA-971++.

Specification Type	*Value*
Bandwidth	100 kHz to 550 MHz at -3dB
Flatness	±0.2 dB, 300 kHz to 400 MHz
Group Delay	Flatness 200 ps up to 400 MHz
Attenuator	36 dB in 2 dB steps
Typical Non-linear Distortion	Better than 1% (400 MHz, output level 300 mV p/p single-ended)
Filters	4 low pass or programmable filters (custom cut-off frequencies for low pass filters up to 400 MHz). High/band pass filters are available for popcorn noise measurement
Differentiators	Two slots for custom modules with data ranges from 5 to 250 Mflux/s (optional)

Table 5 ANA-971++ Specifications

3.2.2 Spectrum Analyzer Specifications

The following specifications define the spectrum analyzer.

Specification Type	*Value*
Bandwidth	500 kHz – 400 MHz
Accuracy	±0.2 dB with 70 dB dynamic range
Selectivity	100 kHz at –3 dB; 500 kHz at –60 dB
Video Bandwidth	Selectable between 100 kHz and 10 kHz
Noise Floor Level	Better than –80 dB

Table 6 Spectrum Analyzer Specifications

3.2.3 PRML Recording Channel Chip Integration Specifications

The following specifications define the ANA-971++ PRML recording channel chip integration.

Specification Type	*Value*
Constructiveness	Plug-in Chip Adapter module in the ANA-971++
Data Rate	Up to 800 Mbit/s (limited by the particular PRML chip capability)
Analog Bandwidth	100 KHz to 550 MHz at –3 dB

Table 7 PRML Recording Channel Chip Integration Specifications

NOTE: Commercial PRML chips from Lucent Technology, Cirrus Logic, Data Path, Siemens, IBM, Marvell, NEC, STMicroelectronics, SSI and others are integrated into the ANA-971++ via an optional daughter board. Each chip requires a separate daughter board. These optional boards are currently available for order from Guzik Technical Enterprises. Additional chips can be integrated on request. The default deliverable production standard is Lucent's Venom (MS231). More information is available on the Guzik web site: www.guzik.com.

3.3 Other Test System Component Specifications

Some other test system components are specified here.

3.3.1 Universal Preamplifier 7 and Universal Interface 7 Specifications

The specifications for the universal preamplifier and interface are defined below:

Specification Type	*Value*
Bandwidth	0.1 to 550 MHz at –3 dB
Flatness	0.3 to 400 MHz ±0.2 dB
Group Delay	Flatness ±100 ps up to 400 MHz
Nominal Output Level	300 mV p/p single-ended
Programmable Attenuator	28 dB in 4 dB steps
Typical non-linear distortion	Better than 1% (400 MHz, output level 300 mV p/p single-ended
Amplification Calibrator Accuracy	2%
Write Current	Programmable from 0 to 80 mA in 0.02 mA steps
MR Read Bias Current	Programmable from -20 mA to +20 mA in 0.01 mA steps for Guzik MR amplifiers; 0-80 mA for MR head amplifiers with direct analog control of bias current; IC dependent for head amplifiers with serial interface control

Table 8 Universal Preamplifier 7 & Universal Interface 7 Specifications

3.3.2 Guzik TSA Type Read/Write MR Amplifier

This special amplifier expands read/write characteristics beyond the limitations of the existing commercial head amplifiers and does not contain any head amplifier IC. It consists of the write driver and the read am-

plifier. (Specifications for amplifiers based on commercial ICs can be found in the corresponding IC's data sheets.) Contact Guzik Technical Enterprises for a complete list of currently available read amplifiers, or check the Guzik web site: www.guzik.com.

3.3.2.1 Read Amplifier Specifications

The specifications for the read amplifier are presented below.

Specification Type	*Value*
Type	Differential, voltage sense
Bandwidth	More than 400 MHz at –3 dB
Flatness	.3 to 350 MHz ±.5 dB
Input Noise	1.1 nV / $\sqrt{\text{Hz}}$
Amplification	130 (nominal)
MR Bias Current	Programmable from –20 to 20 mA in 0.01 mA steps
Common Mode Rejection Ratio	Better than 28 dB at 500 MHz

Table 9 Read Amplifier Specifications

3.3.2.2 Write Driver Specifications

The specifications for the write amplifier are presented below.

Specification Type	*Value*
Write Data Rate	More than 800 MHz
Rise/Fall Time of Write Current (10%-90%)	Less than 800 ps (current 50 mA, L=70nH sequentially with R=20 Ohms)
Write Current	Programmable from 0 to 70 mA (zero to peak) in 0.02 mA steps (0 to 100 mA version is available)
Write to Read Switching Time	Less than 1.5 µs
Head Voltage Swing	More than 20 V peak to peak

Table 10 Write Driver Specifications

CHAPTER 4

HARDWARE COMPONENTS

4.1 RWA-2550++

The RWA-2550++ contains electronic circuits that provide the measurement capability, along with communication with the host computer and control of the ANA-971++.

This component cannot be opened without invalidating the Guzik Technical Enterprises warranty. Therefore, a further description of the internal components is necessary.

4.1.1 Bit Shift Analyzer

An optional **bit shift analyzer** board can be installed in RWA-2550++. This board must be installed by Guzik Technical Enterprises Manufacturing prior to delivery of the system.

4.2 ANA-971++

The ANA-971++ provides analog processing of the read back signal.

4.2.1 Main Internal Components

The ANA-971++ consists of the following:

- a **variable attenuator**
- a **filter** matrix with four slots for filters
- one or more **filters** to place in the filter matrix slots
- a **read channel** with a **peak detector**, **comparators** for PW measurements and data qualification (used in peak detector mode)**,** and one of two software-selectable **differentiators** that provide digital data pulses at the peaks of the read back signal.
- a **spectrum analyzer** is used by some tests to perform measurements in frequency domain
- a **PRML chip adapter interface** board receives the analog signal after attenuation and filtering providing error rate measurements through different types of PRML chips on **PRML chip adapter daughter boards**, one for each PRML chip. Contact Guzik Technical Enterprises for a complete list of currently supported PRML chip adapter daughter boards.

Figure 5 shows the ANA-971++ components in a block diagram.

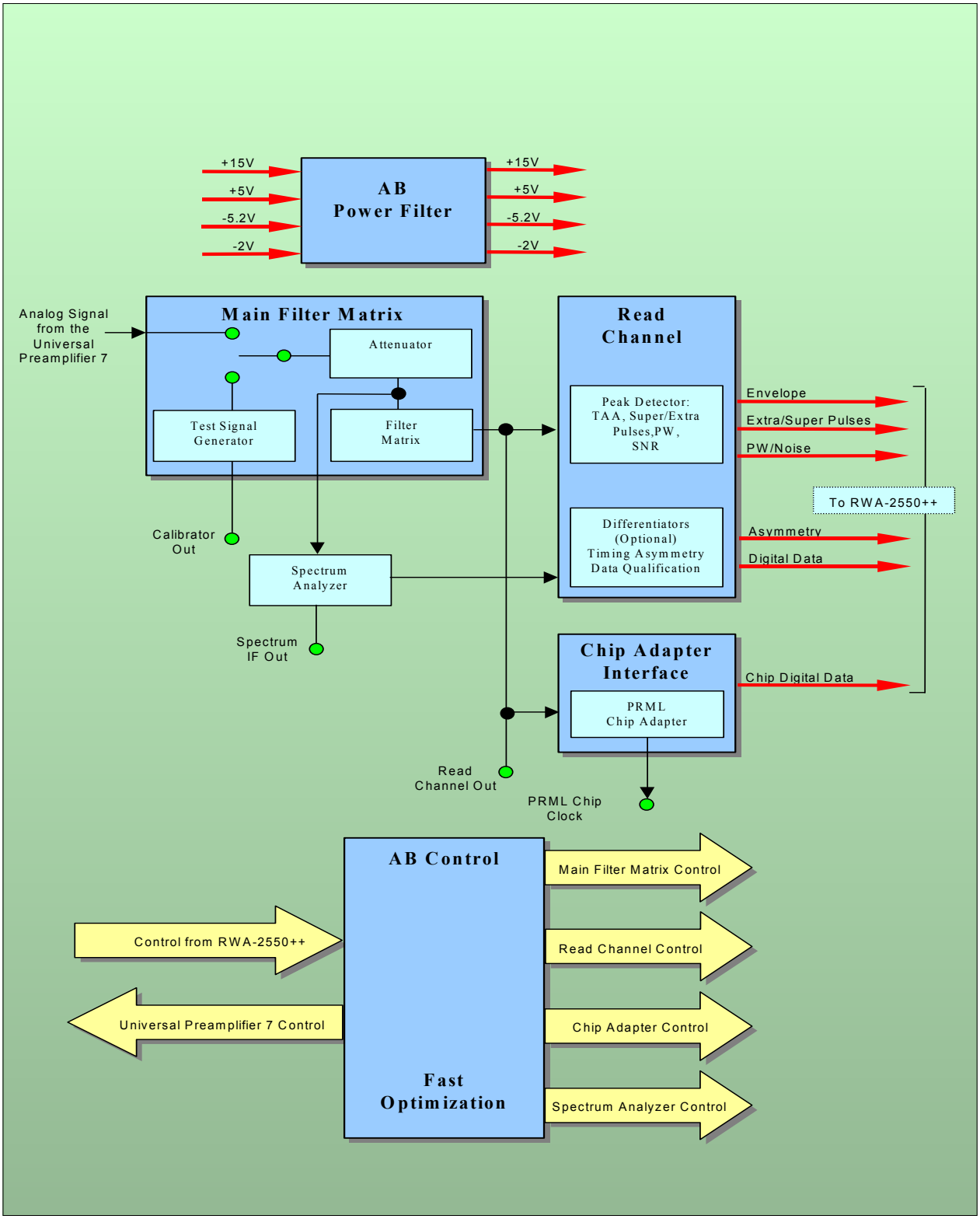


Figure 5 ANA-971++Block Diagram

4.2.2 Filters

The **Filter Matrix** has four slots, where different low-pass (or high-pass/band-pass for the Popcorn Noise Measurement) **filters** are installed to provide the required bandwidth of the ANA-971++.

All analog measurements (except those performed through the Spectrum Analyzer), and all digital measurements are performed by processing analog signal passed through one of these filters.

Filter selection is performed by software.

These filters are custom-made by specifications provided by the user. The following options are available:

- 3 or 5 pole
- Bessel or Butterworth filters with cut-off frequencies up to 400 MHz
- a programmable filter, with software-controllable cut-off frequency and boost is available (currently, SSI 8101 is one programmable filter integrated into the ANA-971++)

The four filter positions are assigned the following names: Parametric (F0), F1, F2 and F3 respectively. The filter in position #0 is always used while adjusting main attenuator. That's why we recommend customers to put into this slot the filter with the highest bandwidth.

4.2.3 Spectrum Analyzer

The **spectrum analyzer** is used by tests that require analysis in frequency domain. The tests include the overwrite test, spectrum analysis, signal-to-noise (SNR) by spectrum method, NLTS based on spectrum elimination approach (5th harmonic method), partial erasure, and others.

NOTE: The spectrum analyzer is connected after the attenuator, but before the filter matrix, to provide measurements in the full frequency range without limiting it by the installed filters.

4.2.4 PRML Chip Adapter Interface

The **PRML chip adapter interface** is used to integrate the PRML chip adapter daughter board into ANA-971++. There is a single slot on the **chip adapter interface board** with two connectors where a **PRML chip adapter daughter board** can be installed.

There are many different types of PRML chip adapter daughter boards, one for each type of PRML chip.

Each PRML chip adapter daughter board provides the ability to perform comparator error and comparator error rate tests for the digital data recovered from the analog signal by the PRML chip.

Fast optimization can be used to achieve best performance. During optimization, the software adjusts PRML chip parameters along with the read/write channel parameters to minimize error rate. The average optimization time varies from 5 to 10 seconds depending on initial conditions, the quality of the signal, and of the particular PRML chip used.

4.2.5 Differentiators

In the read channel there are 2 slots for installation of user-specified **differentiator** modules. There are five differentiator modules designed to be used within different frequency ranges: 5-10 MFlx, 10-30 MFlx, 30-50 MFlx, 50-100 MFlx and 100-160 MFlx. Differentiators for higher frequencies are available by customer request. For more information contact Guzik Technical Enterprises.

4.3 Universal Preamplifier and Universal Interface Boards

To work together with a spinstand, the RWA-2550++ is shipped with a **universal preamplifier 7** and **universal interface 7**. The two boards connect the RWA-2550++ to different types of head amplifiers. They control the read/write signals, write and read bias currents, condition write data signals and analog read data, and provide a serial interface for serially-controllable head amplifier ICs.

The **head amplifier** is a board placed between the universal interface and a head that performs write and read operations.

There are two types of head amplifiers:

- a newer design works with TSA-type heads, and minimizes the length of the connection between the head and the head amplifier (this is achieved by placing the head amplifier directly onto the head cartridge - TSA-type head amplifiers target high frequency applications, having much better frequency response)
- an older design of the head amplifier is placed on the head loader, and heads are connected to it through the pogo pins located on a paddle board

Most head amplifiers are based on commercial head amplifier ICs. More than 100 types of commercial head amplifier ICs are integrated into the RWA. Guzik Technical Enterprises offers a special Guzik MR head amplifier design based on discreet components and supporting very-high-frequency applications beyond the operating range of commercial IC capabilities.

Refer to the *Universal Preamplifier 7 and Universal Interface 7 User's Guide* for more details.

CHAPTER 5

TEST SYSTEM CONFIGURATION

The RWA-2550++ is used in two main configurations of test systems: Head Stack Assembly (HSA) Tester and Head Gimbal Assembly (HGA) Tester.

5.1 Head Gimbal Assembly Test System

The head gimbal assembly test system is used to test a single head with a single media disk installed on a spinstand. The block diagram below (see Figure 6) shows components of the HGA test system:

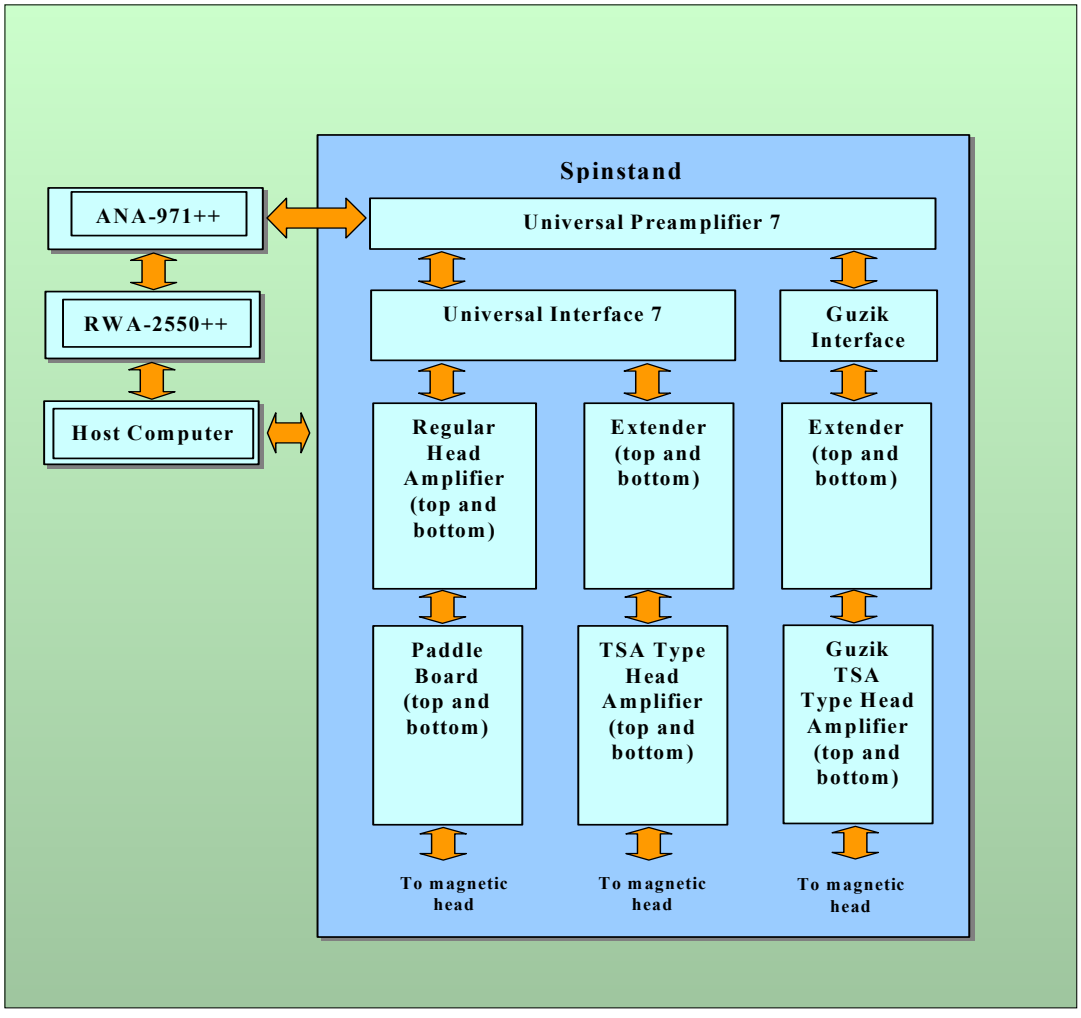


Figure 6 HGA Test System - Block Diagram

The head gimbal assembly option is used to test a single head with a single media unit

5.2 Head Stack Assembly Test System

The block diagram below (see Figure 7) shows components of the HSA test system:

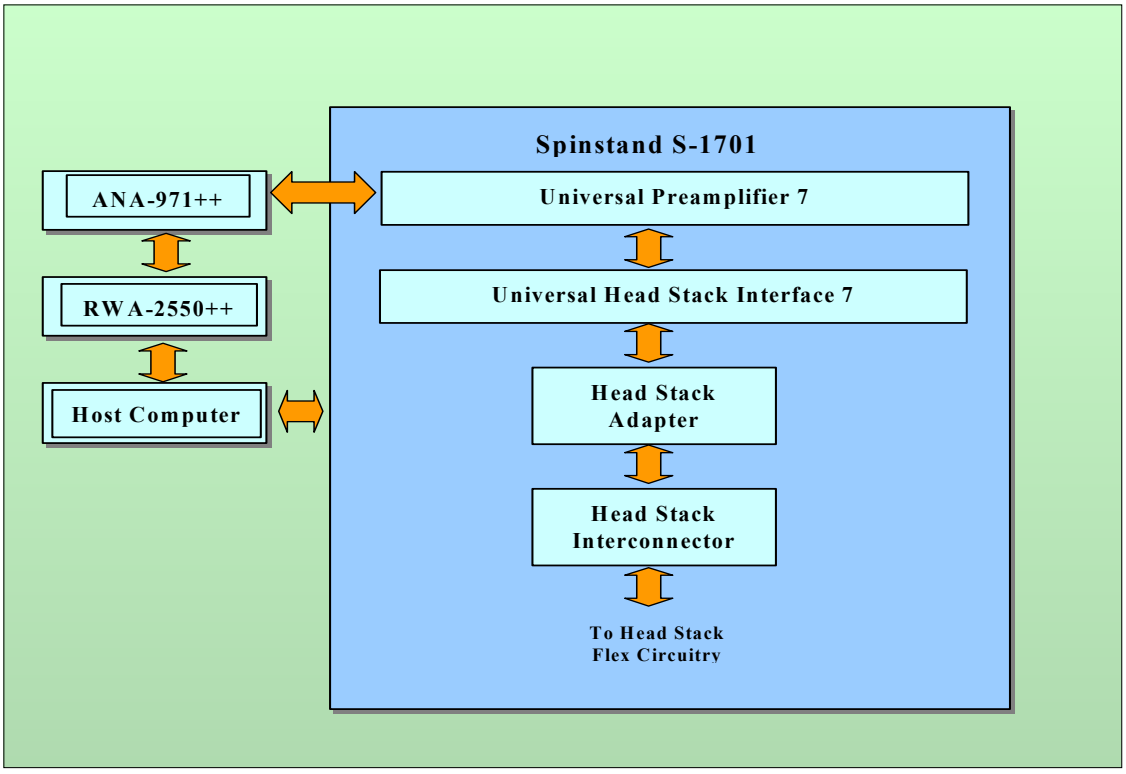


Figure 7 HSA Test System - Block Diagram

The head stack assembly option is used to test a head stack assembly with the disks pack installed on the spinstand.

NOTE: A HAS test system can be installed on a S-1701 spinstand only.

CHAPTER 6

HARDWARE SET-UP

6.1 System Cabling

Figure 8 shows the RWA-2550++ connections for Guzik test systems. There is no installation order for the cabling. A list of the cables follows the diagram.

6.2 Spinstand Connection

Figure 8 shows the RWA-2550++ connections for Guzik spinstand models S312[MP] and S1701[MP]. When making connections, check the cable part numbers carefully.

6.3 Grounding

The RWA-2550++ and the ANA-971++ have ground posts. Ground straps (cables) are supplied with every RWA-2550++ system.

Connect grounds between the RWA-2550++, the ANA-971++ and the spinstand.

CAUTION: Be sure not to form a loop in the ground connections.

6.4 Power

The RWA-2550++ model can operate from alternating current (ac) input in the range from 100 to 230V.

No manual selection of the input voltage is required.

CAUTION: Never make any connections between a RWA-2550++, a ANA-971++, or a spinstand when the power is ON. The result can be a serious damage to all or some of the system components.

No special sequence is required to power-up the entire RWA test system or its components.

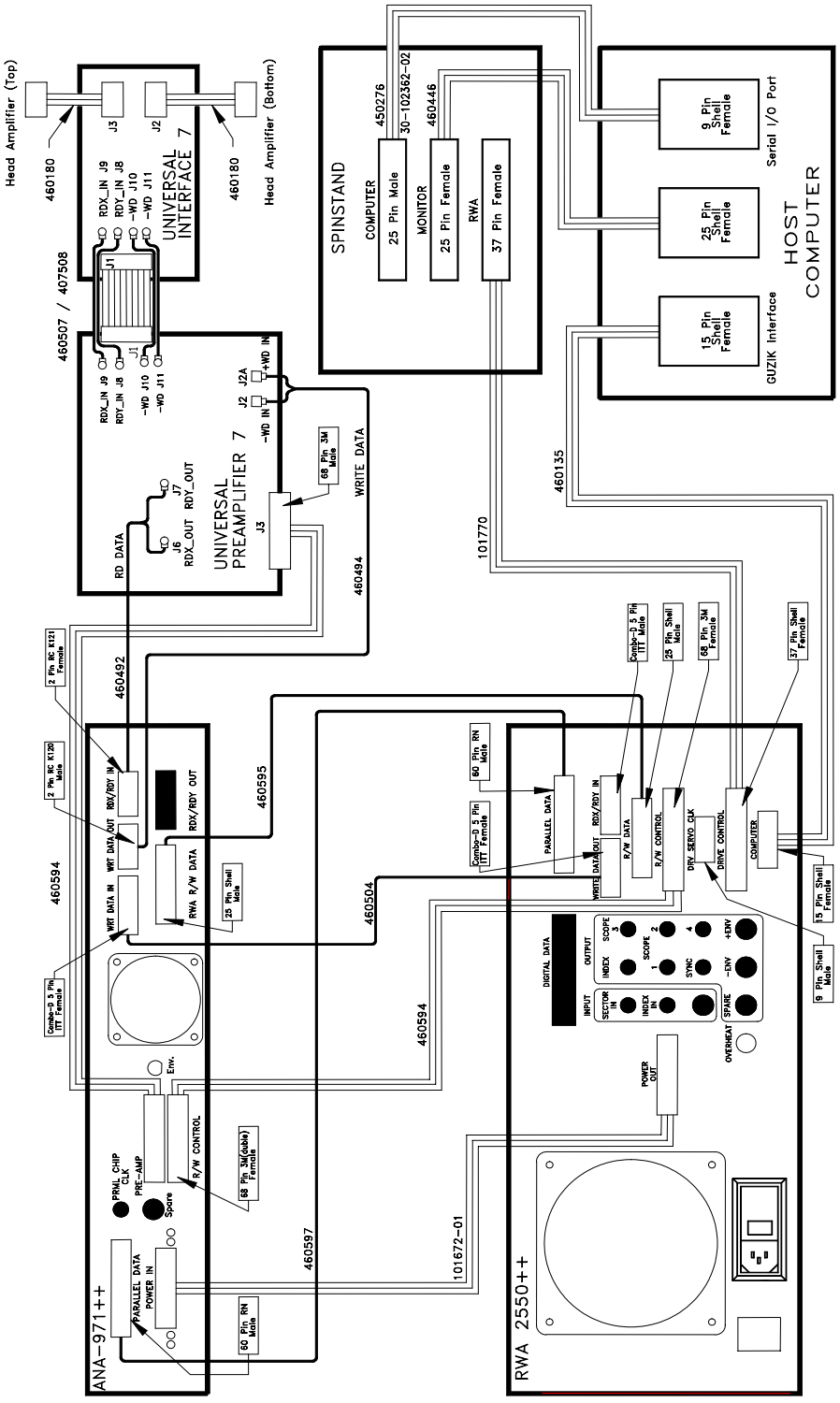


Figure 8 A Test System External Cabling Diagram

6.5 System Cables

Cable Name		*Description*
AB Power Cable	P/N:	460597-A
	From:	RWA-2550++ <Power Out>
	To:	ANA-971++ <Power In>
	Type:	4+5 D-Shell
R/W Control Cable	P/N:	460594-A
	From:	RWA-2550++ <R/W Control>
	To:	ANA-971++ <R/W Control>
	Type:	68 pin 3M
Computer Interface Cable	P/N:	460135-C
	From:	RWA-2550++ <Computer>
	To:	Guzik Host Adapter board in a host computer
	Type:	15 pin M to 15 pin M
R/W Data Cable	P/N:	460595-A
	From:	RWA-2550++ <R/W Data>
	To:	ANA-971++ <RWA-2550++ R/W Data>
	Type:	25 pin F to 25 pin F
Read Signals Cable	P/N:	460492-A
	From:	ANA-971++ <RDX/RDY In >
	To:	Universal Preamp 7/2550 J6, J7
	Type:	2 pin RC K120 M to 2 SMB
Parallel Data	P/N:	460597-A
	From:	RWA-2550++ <Parallel Data>
	To:	ANA-971++ <Parallel Data>
	Type:	60 pin RN F
Write Data Cable	P/N:	460494-A
	From:	ANA-971++ <Wrt Data Out >
	To:	Universal Preamp 7/2550 J2, J2A
	Type:	2 pin RC K121 F to 2 SMB
Preamp Cable	P/N:	460594-A
	From:	ANA-971++ <Pre-Amp>
	To:	Universal Preamp 7/2550, J3
	Type:	68 pin 3M F
Universal Interface Cable	P/N:	460507-L for s312[MP] and 460508-E for s1701[MP]

	From:	Universal Preamp 7/2550, J1, J8-J11
	To:	Universal Interface 7/2550, J1, J8-J11
	Type:	Coax + flat ribbon assembly
Drive Control Cable	P/N:	450198-B
	From:	RWA-2550++ <Drive Control>
	To:	spinstand <RWA>
	Type:	37 pin shell M
Computer/Spinstand Cable	P/N:	102362-A
	From:	A host computer 9 pin serial I/O port
	To:	spinstand <Computer>
	Type:	25 pin shell M
Grounding Cables	3 grounding cables are provided.	
BNC/BNC Cables	4 of these cables are provided for diagnostic use with an oscilloscope, network analyzer, etc.	
Power Cable	1 AC power cable is provided for the RWA	
BNC/SMB	1 cable is provided for connection between the signal generator and the Head Calibrator board for calibration purposes.	
BNC/MCX	1 cable is provided for connection between the analog read signal test point on the UP-7/2550 to an oscilloscope for diagnostic purposes.	

Table 11 System Cable List

CHAPTER 7

INSTALLATION OF DAUGHTER BOARDS

Daughter boards are installed into the ANA-971++. Figure 9 shows an inside view of the ANA-971++ from above, with the front panel at the bottom. See Figure 10 for a photograph of the same view.

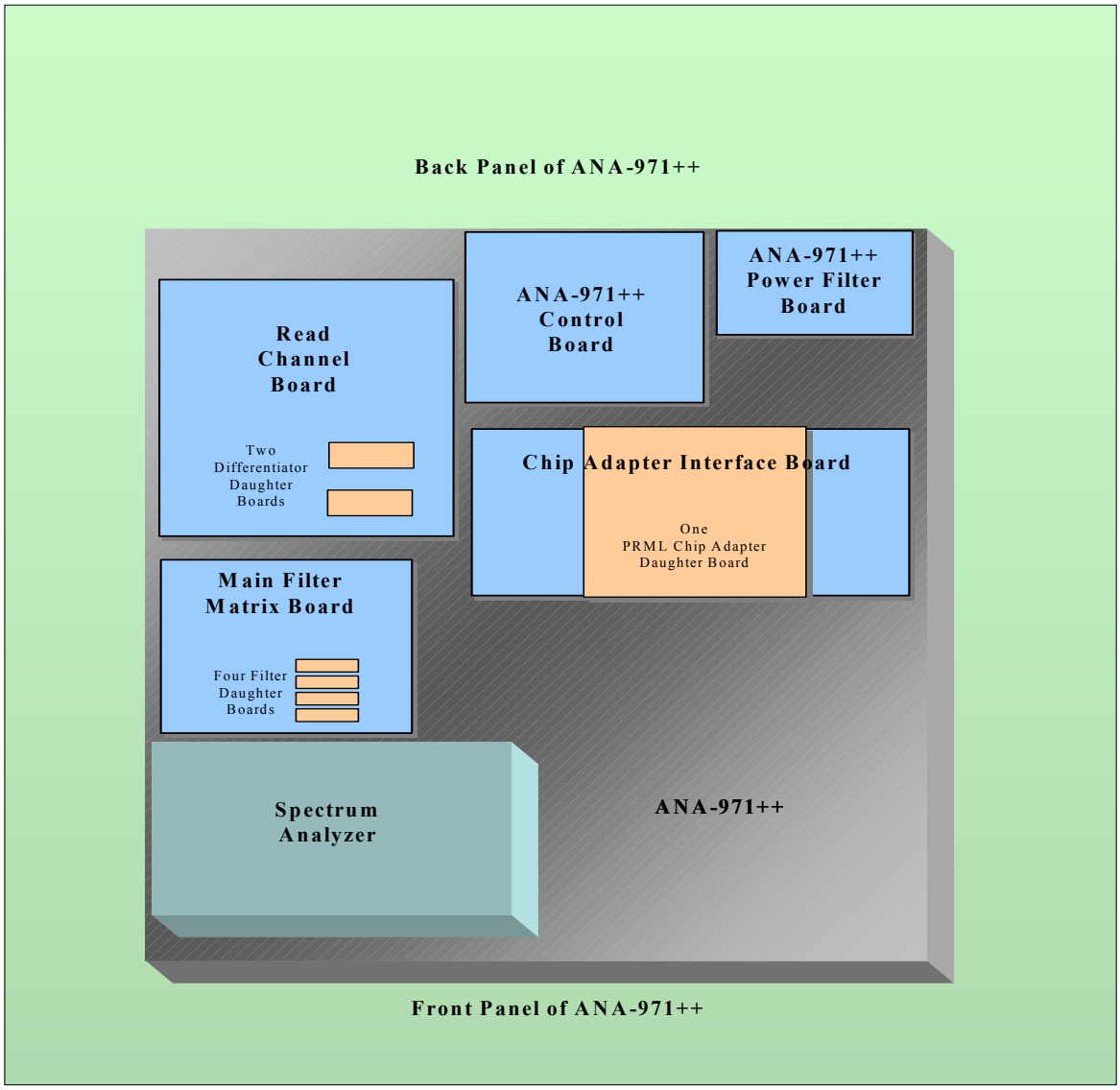


Figure 9 Layout Diagram of the ANA-971++

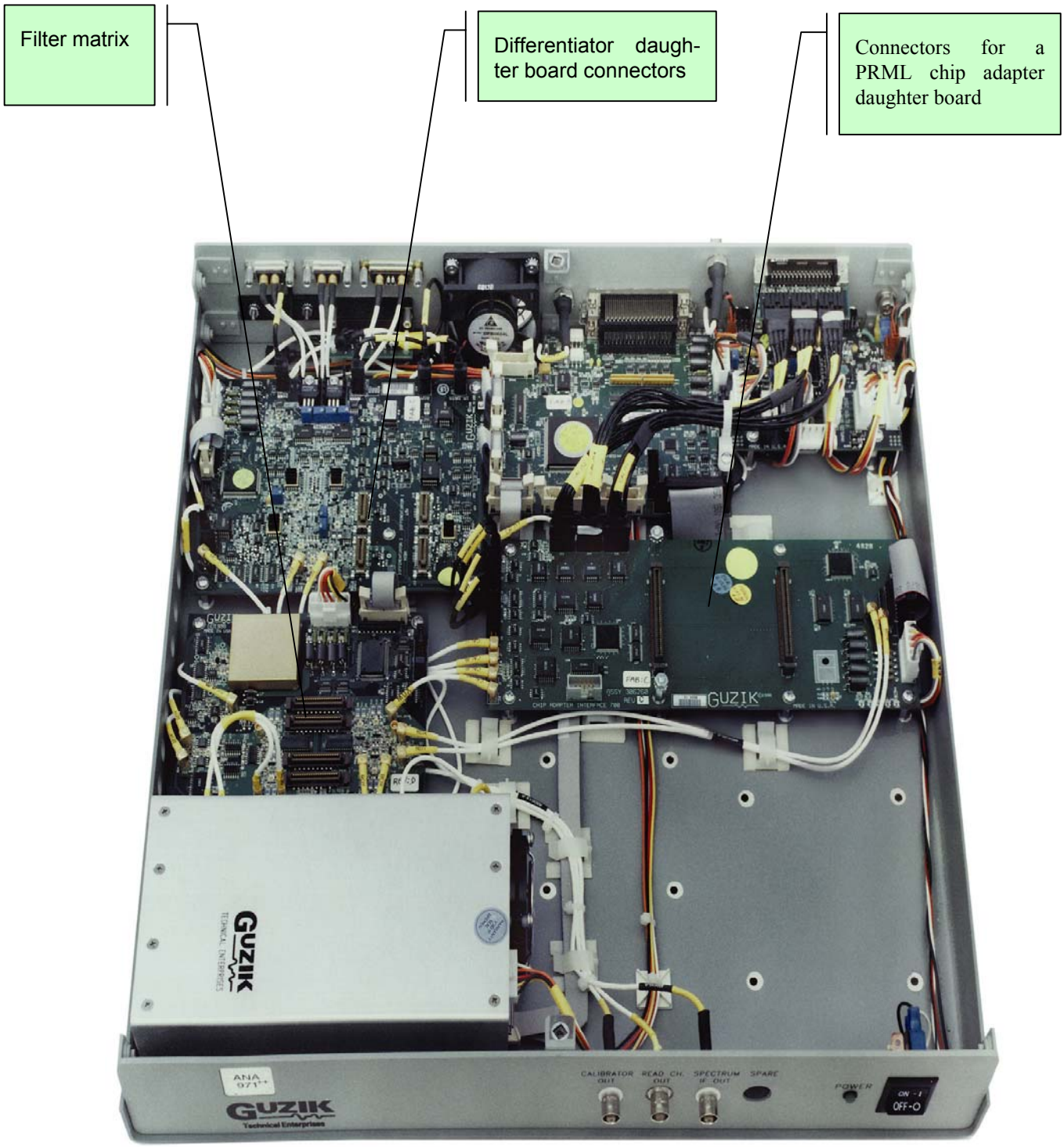


Figure 10 Layout Photograph of the ANA-971++

7.1 Installation of PRML Chip Adapter Boards

There are many variations of PRML chip adapter boards available from Guzik. The form factor of all PRML chip adapter boards is exactly the same, and the installation onto the PRML chip adapter interface (CAI) board is performed in the same manner.

All PRML chip adapter boards are installed on top of the PRML chip adapter interface (CAI) board. This board is located to the right front of the ANA-971++ (see Figure 9)The PRML CAI board has two open female connectors that match the male connectors on the underside of the PRML chip adapter daughter board. The PRML chip adapter daughter board and PRML CAI board connectors are keyed, so that there is only one orientation where mating is successful.

1. Take appropriate static electricity precautions.
2. Turn off power to the unit.
3. Position the ANA-971++ with the front panel of the unit facing you.
4. Grip the PRML chip adapter daughter board by spanning the board with your hand and pressing on the left/right edges of the board.
5. Position the PRML chip adapter daughter board over the CAI board with the board name (printed on the side of the PRML chip adapter daughter board) on your left side. (There are one or more older Guzik PRML chip adapter daughter boards where the name is not on the left side, but the part number of the board is on the left side. Also, there are always a group of four gold cable connectors on the right side of the PRML chip adapter daughter board.)
6. Press the PRML chip adapter daughter board slowly but firmly down onto the two connectors, ensuring that there is equal down force applied to both connectors simultaneously.
7. Attach the I/O cables to the appropriate pins on the chip adapter board according to the cable labels.
8. Tighten nuts on the supporting stand-offs.

7.2 Installation of Filter Boards

Filter boards are small, less than 2" x 1, with only one connector on one edge of the board. All filter boards available from Guzik have the same form.

Refer to Figure 9 for the layout of the ANA-971++. All filter boards are installed on top of the main filter matrix (MFM) board. This board is located to the left front of the ANA-971++. The board has four open female connectors that match the male connectors on the side of the filter board. The filter and MFM board connectors are keyed, so that there is only one orientation where mating is successful.

The filter positions are numbered **0 to 3** as shown in Figure 9.

The programmable filter can be installed in any slot except slot 0 (this is a software limitation, not a hardware limitation). You can use only one programmable filter at a time.

CAUTION: Slot 0 must be occupied or software problems can occur at or after its start. The controlling software will not initialize without a filter in slot 0. Some precautions must be taken on the filter installed in the slot #0. The main attenuator adjustment is always performed through this filter. If cut-off frequency of the filter installed in this position is less than the highest frequency component of the input signal, attenuator will be set to a wrong position that will result in the read channel saturation and wrong measurements. Guzik recommendation is to put into this slot a filter with the highest cut-off frequency among those four that are supposed to be used with this set-up.

Refer to the *WITE User's Guide* for instructions on how to select and control the programmable filter. The WITE software provides a convenient way to set filter characteristics (cut-off frequency and boost) for each zone in the set-up.

1. Take appropriate static electricity precautions.
2. Turn off power to the unit.
3. Position the ANA-971++ with the front panel of the unit facing you.
4. Grip the filter board by spanning the board with your fingers over the long axis of the board.
5. View the filter board, and notice that the connector is not as long as the filter board, and there is a tab of IC board beyond the connector. Orient the tab to your left side, with the male connector pointed down.
6. Position the filter board over the MFM board.
7. Press the board slowly but firmly down onto the female connector.

When removing a filter, do not pinch the board in the middle and pull it out (there are sharp objects on some boards, and you could damage components on the board). Span the length of the board, and place your fingers only on the edges of the board.

NOTE: Filter 0 slot must always be filled, and usually with the Open Filter.

CAUTION: Be sure that the filter with the highest bandwidth is in the slot #0.

7.3 Installation of Differentiator Boards

Optional differentiators are located in the read channel board located in the ANA-971++. The differentiators' positions are named HIGH and LOW. These are the names of the differentiators used by software for selection. These names are traditional and do not have any other meaning, but designating the slots. The connectors on the differentiator board are keyed such that they cannot be installed in a wrong way.

Differentiator boards are small, less than 3" x 1.5", with two male connectors on one side of the board. All differentiator boards available from Guzik have the same form.

Refer to Figure 9 for the layout of the ANA-971++. All differentiator boards are installed on top of the read channel (RC) board. This board is located to the left rear of the ANA-971++. The board has two open female connectors that match the male connectors on the side of the differentiator board. The differentiator and RC board connectors are keyed, so that there is only one orientation where mating is successful.

Take appropriate static electricity precautions.

1. Turn off power to the unit.
2. Position the ANA-971++ with the front panel of the unit facing you.
3. Grip the differentiator board by spanning the board with your fingers over the long axis of the board, and position the board with the connectors pointed down.
4. Position the differentiator board over the RC board.
5. Press the board slowly but firmly down onto the female connectors.

NOTE: When removing a differentiator, do not pinch the board in the middle and pull it out (there are sharp objects on some boards, and you could damage components on the board). Span the length of the board, and place your fingers only on the edges of the board.

CHAPTER 8

SOFTWARE INSTALLATION AND REQUIREMENTS

8.1 Host Computer Installation

WITE is a complete engineering and production software package to be used with the RWA-2550++. WITE is installed onto the host computer and is licensed for use with a specific RWA or several RWAs. For detailed installation instructions, refer to the Guzik publications *WITE User's Guide,* volumes 1 and 2, the *WITE Developer's Kit Programmer's Reference Guide***,** and the *PRML/NLTS Tests User's Guide*.

8.2 Host Computer Hardware Requirements

A host computer controls the RWA sub-system. The host computer communicates to the RWA-2550++ via the Guzik host adapter board installed in an ISA expansion slot in the host computer.

The host computer conforms to several configuration requirements. The minimum hardware configuration of the host computer is as follows:

- IBM PC/PC clone, Pentium class or better (Pentium II is recommended)
- one available ISA slot
- Microsoft Windows 95, 98
- 32 MB RAM (at least 64 MB recommended)
- at least 500 MB of free space (recommended 2GB drive)
- CD ROM drive
- VGA graphics board with at least 800 x 600 resolution
- mouse
- monitor capable of at least 800 x 600 resolution

NOTE: Guzik sells an optional host computer for test systems. This pre-configured host computer is completely compatible with the RWA-2550++ hardware and software. Any non-Guzik host computer should be thoroughly tested for compatibility with the RWA-2550++ system.

CHAPTER 9

CALIBRATION

9.1 RWA-2550++ Calibration

The RWA-2550++ requires calibration when:

- a new RWA-2550++ System is installed
- installation of Guzik software has been performed
- there is a change in the environmental conditions
- the data rate is changed
- rotational speed (RPM) is changed
- time constant of peak detector is changed
- it is the scheduled time to perform routine calibration
- there is a change in the hardware configuration (filters, preamplifiers, differentiators, etc.)

Calibration of the system consists of precomp calibration, peak detector calibration, TAA calibration, current calibration, MR impedance calibration (optional), bit shift calibration (optional).

9.2 Required Equipment for Calibration

The equipment required for calibration purposes is listed below:

- one current probe, 100mA range, 1mA resolution
- one oscilloscope with full (not at -3dB) bandwidth response 400MHz
- one head simulator (resistor and jumper)
- one sine wave signal generator (400MHz range, 0.2% stability, and 0.5% amplitude calibration)
- one head calibrator board and cable

The equipment required for each particular calibration is listed in each procedure description.

9.3 Write/Bias Current Calibration

The RWA-2550++, in configuration with the Universal Preamp 7requires neither write, nor read bias current adjustments. The UP-7, the UI-7, and the head amplifiers are calibrated by Guzik manufacturing.

In general, to check the read bias current accuracy, connect the 20-Ohm resistor instead of the read element, start software, and set the required current value and measure voltage with an accurate multimeter. The actual bias current is equal to the measured voltage divided by 20.

NOTE: Be sure that 20-Ohm resistor you are using is accurate (better than 1% tolerance).

To check the write current accuracy, connect the 20-Ohm resistor instead of the write element, put the current probe on it, and start continuous write operations in software (see *WITE User's Guide*). Measure the peak-to-peak value of the current with the scope. Actual current is equal to half of the measured value, because the last one gives you peak to peak value from current flowing in one direction to current flowing in the opposite direction.

The same approach can be applied to check bias and write current in the head stack.

NOTE: There is a possibility to recalibrate bias and write currents in a field. Please contact Guzik Technical Enterprises for details.

9.3.1 Current Calibration Required Equipment

The following equipment is required to perform this type of calibration:

- one current probe, 100 mA range, 1 mA resolution, 100 MHz bandwidth (or higher)
- one oscilloscope with 400 MHz bandwidth full response (not at -3dB)
- one 20 Ohm resistor with a tolerance better than 1%
- one multimeter

For more details see the *Universal Preamplifier 7 and Universal Interface 7 User's Guide*.

9.4 TAA Calibration

For absolute TAA measurements, TAA calibration is performed by applying a known signal from a generator to the input of the head amplifier. Alternatively, the TAA can be normalized to the signal produced by any reference disk/head combination.

In both cases, the objective is to calibrate the gain of the entire read path, beginning at the first accessible signal point so that the TAA voltage measured through the RWA-2550++ equals the actual average voltage at the input.

The read path consists of (see Figure 11):

- the read amplifier in the write/read IC on the head amplifier board
- the amplifier on the universal interface board (there are two of them, one per each head)
- the amplifier and the attenuator on the UP-7
- the read channel filter (one of four) or the spectrum analyzer in the ANA-971++
- the peak detector circuit

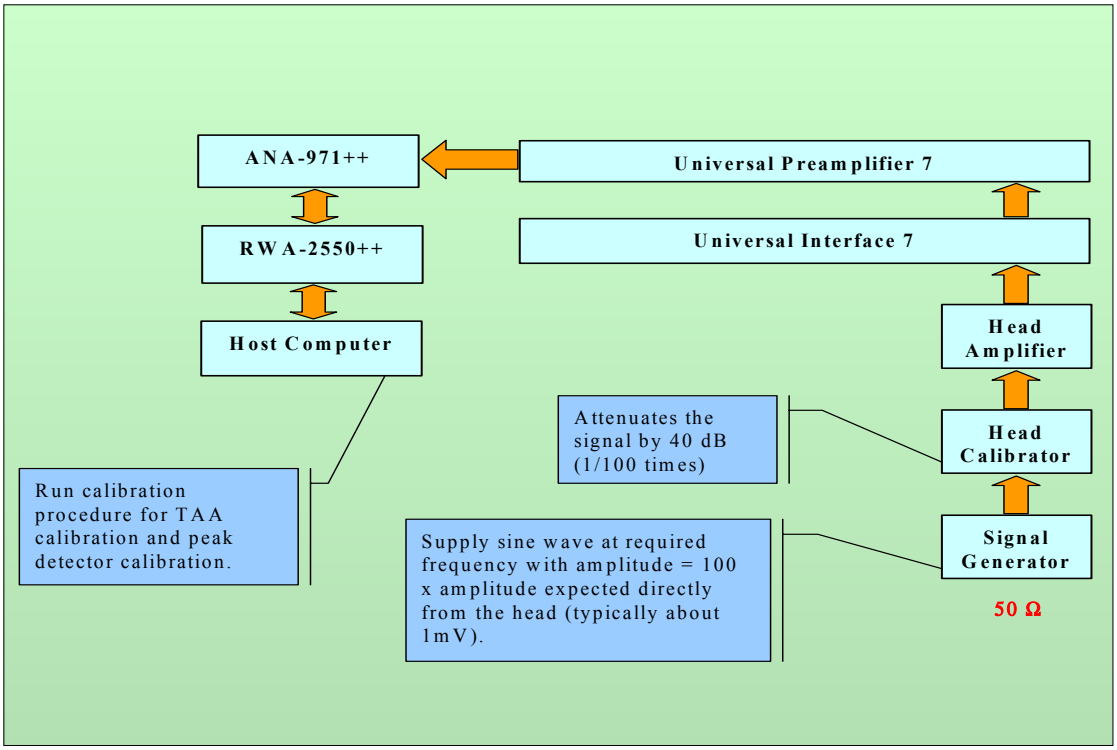


Figure 11 TAA Calibration for the Universal Preamplifier Configuration

NOTE: There are two channels for Head 0 and Head 1. They must be calibrated separately for TAA, but separate calibration is not required for peak detection.

TAA calibration is performed in software for each head channel individually. Refer to the software manual for the details regarding this procedure.

The gain calibration of the entire read channel is done automatically for each of the four main filters (including the spectrum analyzer), but only for the **currently programmed** settings of the programmable filter. The result of calibration is a set of coefficients that are to be applied depending upon through which filter and for which head TAA measurement is being performed. These coefficients are stored in the product set-up.

TAA must be re-calibrated after any changes in:

- data frequency
- head amplifier board (except of the TSA type)
- universal interface 7 or/and universal preamplifier 7 boards
- programmable filter setting
- peak detector time constant changes
- quick charge (QC) on/off

Head amplifiers of TSA type used with the UP-7 are calibrated while manufacturing, so they can be replaced at any time without re-calibration

9.4.1 TAA Calibration Required Equipment

The following equipment is required to perform this type of calibration:

- sine wave signal generator, 400 MHz range, ..5% amplitude accuracy.
- head calibrator board and cable

9.5 Peak Detector Calibration

Calibration of the peak detector is required for accurate setting of the **threshold voltage**. The threshold is used for several purposes. It is used in the peak detection type of channel to qualify data pulses. It is used for extra pulse detection. SNR measurement uses thresholds to calculate RMS of noise. PWN measurement uses threshold as well.

Threshold setting in software for all mentioned purposes is expressed in terms of percentage of the envelope level. While calibrating the peak detector, reference value for 100% of the threshold is being determined. The peak detector calibration must be done every time the data frequency or the peak detector time constant is changed, or a pattern is changed, or quick charge (QC) on/off.

Figure 12 is a block diagram of the threshold comparator circuitry. The signal (a) is an analog data, conditioned to a nominal voltage by the system attenuator.

The peak detector (b) produces a low-frequency (DC-500 KHz) voltage (c), which is the envelope of the peaks of the signal (a). The envelope voltage is a function of:

- pulse width and shape
- data frequency

- peak detector charge mode
- peak detector discharge time constant

The DAC (d) is a multiplying DAC which uses the envelope voltage as a reference and outputs it multiplied by a number ≤ 1 set by software. The output of the DAC is the threshold voltage (e). This voltage is applied to a fast comparator (f). The signal (a) is applied to the other input of the comparator. The output of the comparator consists of pulses having high level when the analog read signal exceeds the threshold voltage.

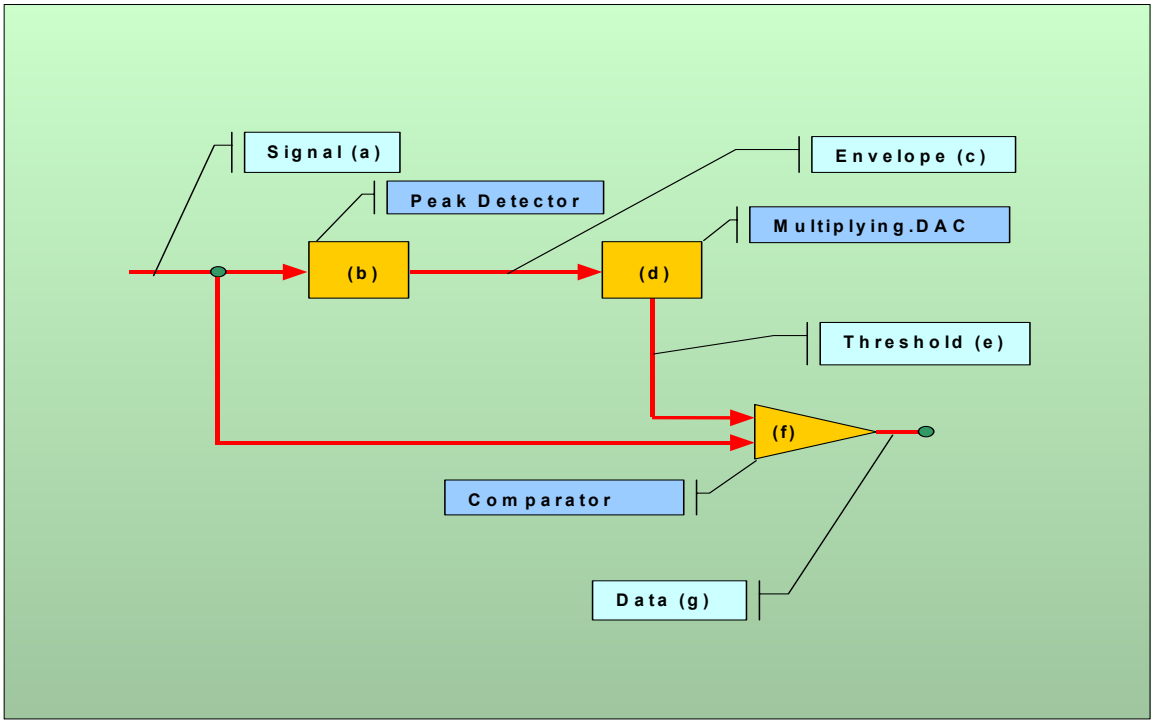


Figure 12 Threshold Comparator Circuitry

The goal of the calibration is to find the DAC setting when the threshold voltage is equal to the peak voltage of the read analog signal (supposing it is **stable**). This setting corresponds to 100% of the threshold, and is used as a reference to set threshold to any other level required by application. In the actual procedure, an externally supplied stable sine wave signal is used. The signal must have amplitude stability better than .25%. The peak detector time constant should be set to a value compatible with the signal frequency. (Refer to Appendix C.) While calibrating, the threshold is adjusted by software until 50% of the pulses trigger the comparator. This is effective because the threshold and the signal are not perfectly stable, and there are amplitude deviations, which are symmetrical around a mean value.

Peak detector calibration is performed by software in most of the cases for the same time as TAA calibration. Refer to the software manual for details about this procedure. The hardware set-up is exactly the same as for TAA calibration and both calibrations are usually performed together.

9.5.1 Peak Detector Calibration Required Equipment

The following equipment is required to perform this type of calibration:

- sine wave signal generator, . 400 MHz range, .5% amplitude accuracy
- head calibrator board and cable

9.6 MR Impedance Calibration

The Universal Preamp 7, the Universal Interface 7 board, and most of the existing head amplifiers provide the capability to measure impedance of MR heads connected to them. This provision may be absent in some particular head amplifiers.

For configurations that have this provision, it is possible to calibrate measurement circuit to improve its accuracy. The software automatically detects the configuration, and either enables or disables running this procedure. The procedure is simple and requires just two different resistors with known resistance measured accurately. Guzik Technical Enterprises recommends using resistors with boundary values for the estimated MR impedance segment. Thus, if the MR impedance is supposed to be between 20 and 40 Ohm, use resistors with these values.

The software asks you to specify these values, and connect resistors one by one to the head amplifier instead of MR head read element. Correction factors are calculated and stored in the set-up. Later they are used while running MR impedance measurement test.

9.6.1 Required Calibration Equipment

The following equipment is required to perform this type of calibration:

- two calibrated resistors with values at the ends of the interval, within which the estimated MR impedance would reside.

9.7 Bit Shift Calibration

The bit shift analyzer optional in RWA-2550++. If it is not installed, or it is installed but not used in the set-up, no calibration is required for bit shift. If the bit shift analyzer is installed, and used for bit shift, and/or error rate measurements in peak detection mode, it must be calibrated. The following is an explanation of what calibrated during this procedure.

The bit shift window is a time interval the RWA-2550++ sets around the center of the data cell. If a data pulse comes within its window, it is correct. If it comes outside its window, margin error is detected. Bit shift window in the RWA-2550++ can be adjusted to different values with the resolution 20 ps. Bit shift test measures number of margin errors for different window sizes building bit shift distribution in this way.

The hardware that controls window size has to be calibrated to provide correct and accurate settings. During calibration, a reference signal with predetermined bit shift value is supplied to the margin error detection circuitry. After that, the window is adjusted such that 50% of the pulses in the calibration signal fall within the window. This window setting is stored as correspondent to the bit shift in the calibration signal. The procedure is repeated for each window size required for the specified data rate. To determine window increment, software divides half of the bit cell width, that is a maximal window size, by 128. The result of the calibration is a table that is stored in the software set-up and used while running bit shift tests.

Bit shift calibration must be done each time a different data rate is set in the RWA. For a set-up with multiple zones, this calibration must be done for each zone. Bit shift calibration is performed internally in the RWA-2550++ without participation of the ANA-971++, and does not require any additional equipment.

Refer to the *WITE User's Guide* for instructions on how to run this procedure.

CHAPTER 10

DIAGNOSTICS

10.1 RWA-2550++ Test Scope Points

Refer to Figure 2, which shows the rear panel of the RWA-2550++.

There are six scope point BNC connectors and 2 input BNC connectors at the RWA's back panel. The input connectors are "Sector In" and "Index In" and can be used to input the corresponding signals from a spinstand or disk drive into the RWA. Both of the signals must be TTL compatible. They are terminated internally in standard Tevenin way (150-Ohm equivalent impedance). If Guzik spinstand is used, these connections are not required.

Scope point BNC connectors are "Index Out", "Scope 1", "Scope 2", "Scope 3", "Scope 4" and "Sync". "Index Out", "Sync" and "Scope 3" are TTL compatible low impedance (50-Ohm) outputs. The rest of the signals are 50-Ohm high frequency outputs with maximum amplitude 800 mV p/p.

"Index Out" is an internal index signal used in the RWA-2550++ for synchronization of all operations.

NOTE: Index Out is **not** a spinstand or a drive index, but it is usually derived from it.

The other scope point signals are software controllable. "Sync" is a data sync point that can be programmed at any data byte in the pattern starting from the address mark (see the *WITE User's Guide* for details). Scope points 1-4 can be set in software to output different signals.

The following tables describe which signals to which scope points can be output.

NOTE: See the *WITE User's Guide* to find out how to make these selections.

10.1.1 Scope Points 1 and 2 Outputs

Output to these scope points could be selected independently but from one and the same set of signals. The difference is that output to Scope Point 2 is gated with the Read Gate during the read operation, while output to Scope Point 1 is direct.

Text	Description
Read Clock	The clock recovered from the read data. This can be the clock from the bit shift analyzer (if it is installed) or from the chip adapter daughter board (if the chip outputs a recovered clock or a system clock).
Margin Error	This signal consists of pulses generated by the RWA-2550++ for every margin error during the bit shift test. This is available only if the bit shift analyzer is installed in the RWA.
~~Super/Extra Error~~	~~Signal from the Analog Box during the super/missing pulse tests, divided in frequency by 2, i.e. each edge of it (falling as well as rising) represents super/missing pulse detection.~~
Super/Extra Error	Signal from the ANA-971++ during the super/missing pulse tests, each pulse represents super/missing pulse detection.
Asymmetry/Noise	Internally generated pulses for noise or asymmetry measurements.
Raw Read Data	Qualified data from the ANA-971++that has not passed yet through the bit shift analyzer data separator. If the latter is not installed, nothing is output.
Read Data	Digital read data either from the bit shift analyzer or from the Chip Adapter if the latter has serial data output or PG NRZ data.

Table 12 RWA-2550++ Scope Points One and Two Outputs

10.1.2 Scope Point 3 Outputs

Text	*Description*
Read Gate	Read gate is used to limit time interval inside of which measurements are to be performed. It can be synchronized either with the read data or with the internal 4 MHz oscillator depending upon which operation is performed.
Write Gate	The write gate is used to gate the write data and write current i.e. only the write data within its duration is actually written. Start and stop timing of the write gate is software controllable.
Address Mark	Internal signal generated by the RWA-2550++ consisting of pulses for every instance of address mark detection.
Sector	Internal sector pulses generated by the RWA. These pulses are of the negative polarity. If external sector mode is used, they are derived from the ones received from a spinstand or a drive.
4 MHz Clock	Internal clock used to provide a proper timing for control signals like the Write Gate.
Write Enable	Internal signal that indicates that write operation is currently being performed by the RWA. This signal enables generation of Write Gate Head 0 and 1.
Index	Internal index generated by the RWA. Can be synchronized with the external index or generated internally. This signal has negative polarity.
Read Operation	Internal control signal generated by the RWA-2550++ to start synchronous read mode, i.e. synchronizing with the read data and address mark detection.
VCO Stopped	Internal control signal used in configuration with the bit shift analyzer only.
ENAMDET (Enable Address Mark Detection)	Internal control signal that enables the detection of the address mark by the RWA. Timing of this signal is programmable in software.
LTD (Lock To Data)	Internal control signal used to switch clock recovery from the internal frequency source to the read data. Timing of this signal is programmable. For the PRML channel, it serves as a "Read Gate" signal for the PRML channel chip.
Read Gate Head 0	The Read Gate if Head 0 is selected, otherwise a logical zero. Actual usage depends on the Universal Preamplifier/Drive Interface Board set-up. This signal has positive polarity.
Read Gate Head 1	The Read Gate if Head 1 is selected, otherwise a logical zero. Actual usage depends on the Universal Preamplifier/Drive Interface Board set-up. This signal has positive polarity.
Write Gate Head 0	The Write Gate signal for Head 0. This signal goes outside RWA-2550++ to the Universal Preamp or Driver Interface board and enables write operation. Actual usage depends upon UP or Drive Interface configuration. This signal has negative polarity.
Write Gate Head 1	The Write Gate signal for Head 1. This signal goes outside RWA-2550++ to the Universal Preamp or Driver Interface board and enables write operation. Actual usage depends upon UP or Drive Interface configuration. This

	signal has negative polarity.
Drive Index	External index from a spinstand or a drive.
Drive Sector	External sector pulses from a spinstand or a drive. This signal has negative polarity.
Clamp	Control signal generated by the RWA-2550++ and used by the Universal Preamplifier board to enable high pass filter during write-to-read transition or popcorn test. This signal has negative polarity. Its timing is controlled by software.

Table 13 RWA-2550++ Scope Point 3 Outputs

10.1.3 Scope Point 4 Outputs

Text	*Description*
Write Data	The actual write data used to toggle the write current direction through the head (except of the special write or erase operations), but not gated by the Write Gate. This data is already precompensated, if precomp is enabled.
Digital Data	External Raw Read Data that is input into RWA-2550++ via connector at the back panel named “External Servo Clock”. This signal can be used in configuration with the bit shift analyzer only.
Calibration Signal	Signal generated by bit shift Calibrator.
Raw Read Data	Internal Raw Read Data (not separated by the bit shift analyzer yet).
PRML Sample Clock	Reserved for future use.

Table 14 RWA-2550++ Scope Point 4 Outputs

NOTE: Not all of the above listed signals may be selected by software in any configuration. See restrictions individually provided with the signal description.

10.2 ANA-971++ Scope Points

There are three scope point BNC connectors on the ANA-971++ front panel. They are named "Calibrator Out", "Read Channel Out" and "Spectrum IF Out". There are two scope point BNC connectors at the back plane of the ANA-971++. They are called "Envelope" and "PRML Chip Clock". All test points except of "Envelope" have 50-Ohm output impedance. "Envelope" signal has 2K-Ohm source impedance. The description of the signals at these connectors is provided in the following table.

Text	*Description*
Calibrator Out	The 8.33 MHz signal from an internal test signal generator
~~Read Channel Out~~	~~The output of the analog channel after attenuation and filtering. The maximum undistorted level is 300 mV p/p. Output greater than this level is either compressed or distorted.~~
Read Channel Out	The output of the ANA-971++ after attenuation and filtering. The maximum undistorted level is 300 mV p/p. Output greater than this level is either compressed or distorted. This may be the analog test output of the PRML chip if Chip Adapter Enabled is selected in the WITE Control menu.
Spectrum IF Out	The output from the Spectrum Analyzer of the intermediate signal at frequency 10.7 MHz. This signal is output after attenuation, so its amplitude does not reflect the level of the signal frequency component to which the Spectrum Analyzer is currently adjusted. The maximum undistorted level is 800 mV p/p.
Envelope	The output of the envelope signal multiplexer. The real-time signal envelope or the signal played back from the envelope memory is selected. An oscilloscope with high input impedance should be used to observe this signal.
PRML Chip Clock	Clock output from the Chip Adapter. It can be either byte clock or bit clock depending upon the particular chip being used. Refer to the chip data sheets to find out which clock is output from it.

Table 15 ANA-971++ Scope Point Outputs

CHAPTER 11

TEST DESCRIPTIONS

11.1 Introduction

In this chapter a number of important tests are described, including:

- Linear tests
- Noise tests
- Track average amplitude and modulation test
- Popcorn noise test
- Stability (Wiggle) tests
- PRML tests
- MR impedance test
- Bit shift analysis tests (requires optional board in RWA-1550++)

11.2 Linear Tests

Linear tests are a set of measurements which determine:

- LF TAA / HF TAA (track average amplitude)
- resolution
- (timing) asymmetry (positive and negative)
- overwrite
- PW50 (pulse width at 50% threshold)

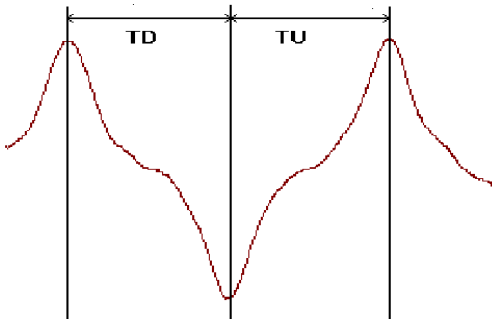
The **LF TAA / HF TAA Test** measures track amplitude. Traditionally, the "lowest frequency" (LF) corresponds to the "100010001000…" pattern, the "highest frequency" (HF) corresponds to the "101010…" pattern. The two patterns are selected in WITE.

A **resolution** is a ratio between HF TAA and LF TAA. The resolution test gives you an idea how pulse interference results in the loss of amplitude at a given data rate.

During the **Overwrite Test** the average amplitude of a recorded user-selectable low frequency signal (usually LF) is measured at the output of the spectrum analyzer, which is adjusted to LF frequency, before and after it is overwritten with a high frequency signal (always HF). The average amplitude before writing the HF pattern is A1 while the average amplitude (through the spectrum analyzer) after overwriting with HF is A2. The result of overwrite test is

$$20 \cdot \log(A1/A2)$$

and is a measure (in logarithmic scale) of the new recording data ability to suppress previously written data. The low (overwrite) frequency is the same as the selected center frequency of the spectrum analyzer.



The (timing) **Asymmetry Test** measures the average difference (in ns) between the distance from a negative peak to the following positive peak and the distance from a positive peak to the following negative peak. Positive or negative asymmetry is defined as the asymmetry, which is measured after positive or negative erasure respectively. Asymmetry measurement is meaningful only on a **LF** signal. Thus,

$$Asymm = \sum_{n=1}^{N} \frac{(TD_n - TU_n)}{N},$$

Where N is number of slope pairs, TD is time between + to – peaks and TU is time between – to + peaks.

Figure 13 Asymmetry Definition

The test algorithm measures negative and positive asymmetry in the following way:

1. The track is DC erased with one direction of flux.
2. LF signal is written.
3. Positive asymmetry is measured.
4. The track is erased in the reverse direction.
5. LF signal is written again.
6. Negative asymmetry is measured.

The **PW50 test (**Pulse Width at 50% threshold) is designed to measure width of an isolated pulses. The test algorithm is as follows:

- the PW pattern is written on the track;
- the virtually isolated pulses of the read analog signal are applied to the comparator with the threshold set at 50%;
- the widths of the pulses are measured.

The accuracy of the pulse width test is sensitive to the setting of the peak detector charge mode and discharge time constant.

The **PWN test** is the average pulse width of a signal written on a media at any threshold level from 0% to 100%. The result is specified in ns. Guzik hardware and software provides a possibility to measure PWN for positive and negative pulses separately.

11.3 Noise Tests

The traditional noise test measures the ratio between the amplitude of a HF signal written on a given track and the RMS value of the signal after the track is erased. The signal-to-noise Ratio (SNR) is calculated using the following formula:

$$SNR = -20 \cdot \log(V_{noiseRMS} / TAA)\, m$$

Where *TAA* is track average amplitude of a HF signal, $V_{noiseRMS}$ is RMS value of a signal on an erased track.

The test optionally can measure the **crest factor**. This is the peak amplitude of the erased signal normalized to the envelope amplitude of a previously written HF signal (in percentage). For an extra pulse on the track, the crest factor is the ratio of the extra pulse amplitude to the HF signal envelope amplitude. These tests are sensitive to peak detector time constant.

Another algorithm of the noise test utilizes the spectrum analyzer to measure signal-to-noise ratio on the signal (without erasure). The algorithm calculates the RMS of the signal harmonics and divides it by the RMS of the background noise, normalized to the spectrum analyzer's video bandwidth.

11.4 Track Average Amplitude (TAA) and Modulation Test

The signal from the head preamplifier is applied through the selected filter and programmable attenuator to the peak detector circuit.

The TAA (track average amplitude) is a running average value of the **peak** voltages in read data (**not** a RMS measurement).

Modulation is measured as the maximum deviation of the reading of digitized envelope from the TAA level in percentage of TAA (see Figure 14).

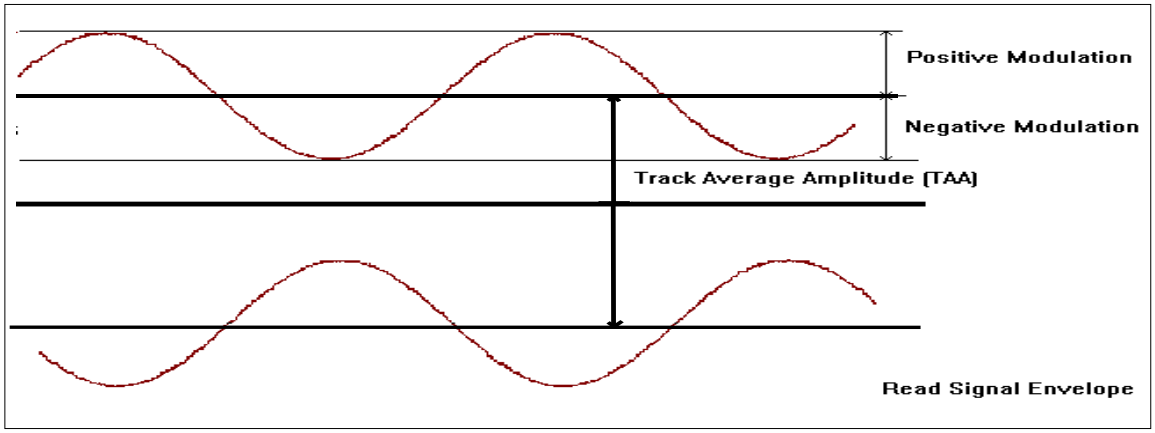


Figure 14 Modulation and TAA

TAA and modulation measurements are also sensitive to the peak detector time constant. The amplitude envelope at the output of the peak detector is digitized every 400 ns (at 3600 RPM) and the values for an entire revolution are stored in the envelope memory.

On each revolution, all samples of the amplitude envelope are processed in real time, so that the values of the TAA and positive and negative modulations are determined at the end of each revolution. The signal envelope on the output of the peak detector is affected by the pulse width of the signal, and by the charging mode/time constant settings of the peak detector itself (see Envelope/Peak Detector Time Constant

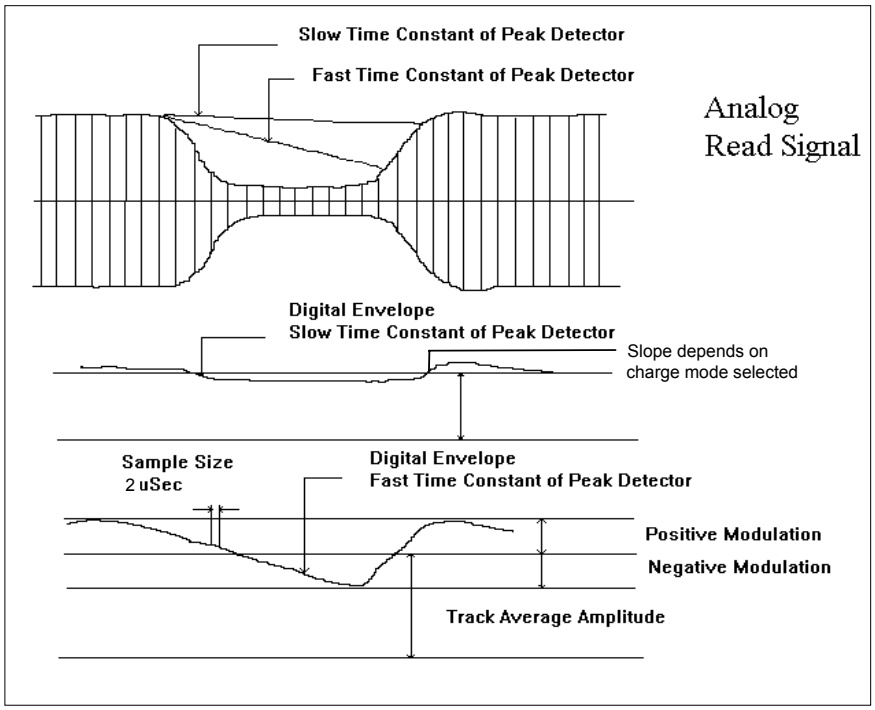


Figure 15 Envelope/Peak Detector Time Constant

The 2.5 MHz sample rate of the envelope memory assures that the recorded envelope will show any peak detector output variation greater than 400 ns. Sampling rate depends upon current RPM and set such, that envelope memory can store all samples for an entire revolution. RWA-2550++ hardware and software provides a possibility to measure TAA for positive and negative pulses separately.

11.5 Popcorn Noise

When a head switches from write to read operation, in some cases it emits random noise spikes which have been named **Popcorn Noise**. The noise spikes are not generally present as written transitions on the disk, but can be detected in the read channel as soft errors.

Popcorn Noise occurs very soon after the switch from write to read operation. The accuracy of measurement of the noise is very sensitive to the write-to-read recovery time of the read-write channel. The recovery time of the Universal Preamplifier 7(UP-7) is 5 µs (typical). Using a high-pass filter with the UP reduces the recovery time to < 3 µs depending on the filter used. These numbers also depend on the head amplifiers. Refer to the Universal Preamplifier manual for details.

The Popcorn Noise has a large high-frequency component; that is, popcorn noise spikes are fast. The filters in the read channel must have a high cut-off frequency in order to provide an accurate Popcorn Noise measurement. A high-pass filter with -3dB cut-off frequency > 1 MHz is usually used. Using a high-pass filter with cut-off frequency too high affects the base noise level, leading to an inaccurate measurement.

The standard algorithm for testing Popcorn Noise in heads is:

1. Write data pulses for a specified amount of time, or a specified number of transitions (1-50K transitions).
2. Stop the write operation and wait for the specified amount of times (5 µs to 3 ms).
3. Read and measure Popcorn Noise.

For details on the measurement method, refer to the *WITE User's Guide*.

11.6 Stability (Wiggle) Tests

Some heads, during write, display a non-repeatable variation in their characteristics, which causes a distorted waveform to be written. This problem varies from head to head. The effects are seen as variations in pulse amplitude, bit shift and pulse width.

There are three stability tests:

1. **Amplitude Stability**: Amplitude variation is measured for many read-write operations
2. **Pulse Width Stability**: Pulse width variation at specified threshold (PWN) is measured for many read-write operations
3. **Error Rate Stability**: Margin errors are counted at a fixed window size for many read-write operations. This test requires optional peak detection channel.

11.7 PRML Tests

Some PRML tests can run on the basic configuration of the RWA-2550++. They are

- comparator error rate
- NLTS spectral elimination

The comparator error test writes data from the pattern generator, or through a PRML read channel chip installed in the chip adapter interface. The data is read and compared with reference to the comparator counting and registering bits in error.

Spectral elimination tests write special periodical patterns of data to the disk, and measure some particular harmonics of the read signal. It occurs that the levels of those harmonics are functions of non-linear transition shift (NLTS). Harmonics are measured using the spectrum analyzer.

For the theory and details of PRML tests, refer to the *WITE PRML/NLTS Tests User's Guide.*

11.8 MR Impedance Test

One of the important MR head characteristics is impedance of the MR element. The RWA-2550++, with the Universal Preamp 7 and most of the Head Amplifiers, provides the possibility to measure it. Actually,

only active resistance is measured in this test (capacitance and inductance can not be measured in this way).

When some head amplifiers are used, this test can not run, because these head amplifiers do not have such provisions. Software automatically detects your configuration and automatically either enables or disables this test.

Contact Guzik Technical Enterprises for information on the head amplifiers compatible with this test.

11.9 Bit Shift Analysis

NOTE: The bit shift analyzer is optional and this test can be run only on the RWA-2550++ equipped with it.

The bit shift analysis is an integral statistical analysis of the bit shift distribution around the center of the data cell. This test measures the timing aperture of a complete write/read system.

The analysis evaluates the integrity of recorded data and the expected error rate in a real-world environment when using peak detection method for data recovery.

For PRML data recovery, some other methods are used to measure error estimation.

To measure bit shift, the RWA-2550++ defines a time window around the center of the data cell. Then, during read, it detects and counts pulses, which fall outside this window. Each event of a pulse falling outside the window is a **margin error**. The **error rate** for a particular window is the ratio of the total number of margin errors to the total number of data pulses read.

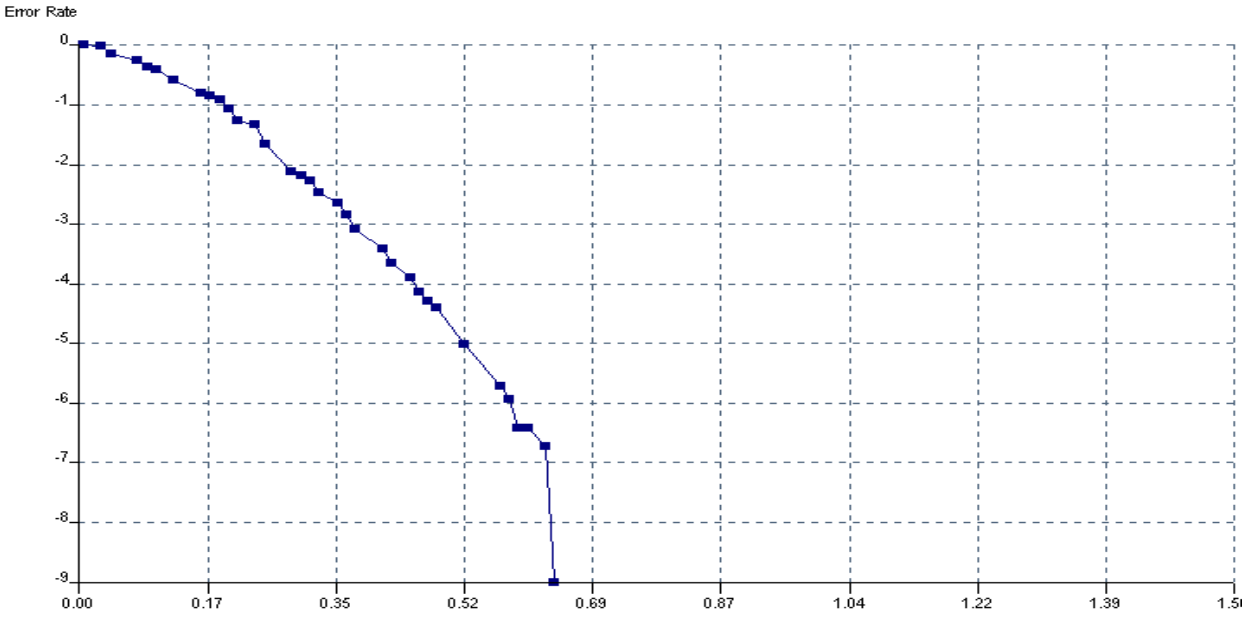


Figure 16 Bit Shift Plot

The bit shift plot produced by WITE shows the error rate as a function of the bit shift window size.

Figure 16 is an example of a bit shift plot. The X-axis represents the distance from the center of the cell to the boundary of the bit shift window. The Y-axis represents the combined error rate for both late and early pulses. Early or late pulses can also be measured independently. The scale for the Y-axis is logarithmic.

For example, a point on the bit shift plot with co-ordinate -6 on the Y axis and 0.57 ns on the X axis indicates that 1 pulse out of 10^6 in the recording system under test is shifted more than 0.57 ns from the center of the data cell.

See the *WITE User's Guide* for more details on the bit shift measurement test.

CHAPTER 12

MAINTENANCE

12.1 RWA-2550++

There is only one part of the RWA-2550++ that requires user maintenance, and only one assembly that is replaceable by the user.

12.1.1 Maintenance

The fan air filter must be cleaned periodically to prevent overheating. This filter is cleaned from the outside of the unit.

The RWA-2550++ enclosure is closed to users. There is a seal on the enclosure, and breaking the seal will void the warranty.

12.1.2 User Replaceable Parts

Fuse Assembly - next to the power cord connector.

12.2 ANA-971++

There is no part of the ANA-971++ that requires user maintenance, and three assemblies that are replaceable by the user.

12.2.1 Maintenance

None.

12.2.2 User Replaceable Parts

The ANA-971++ enclosure is opened for installation and removal of daughter boards:

- PRML chip adapter daughter boards
- differentiator daughter boards
- filter daughter boards

CHAPTER 13

HARDWARE TROUBLESHOOTING

13.1 General Troubleshooting

The following techniques are used to pin-point the cause of most problems. In case of a malfunction, user is encouraged to try using them before contacting Guzik Technical Support.

- all appropriate power switches, indicator LEDs, power cables and control cables should be checked if a device appears to be offline or dead
- all relevant RWA-2550++ and ANA-971++ scope outputs should be checked to see if the expected signals are present (for example, the presence of the read signal can be checked at the ANA-971++ output as well as the Raw Read Data scope output on the RWA-2550++ (Scope 1 and Scope 2)), and the presence of the write data can be checked at the WRT DATA output on the RWA
- check signals at the scope-points on the Universal Preamp 7, also to ensure that the expected signals are present (for example, the presence of the read signal can be checked at the RDX and RDY scope points), and similarly, the presence of differential write data can be checked at the board-end of the write data cable, or the presence of write current can be checked at the head using a resistor and a current probe
- if the problem seems related to a certain piece of hardware (like say the RWA), try exchanging it with another one and see if the problem goes away
- in many cases the problem can be solved simply by rebooting the system, i.e. switch off power to all devices and switch it back on; also reboot computer

13.2 RWA 2550++ Power Troubleshooting

In case of overheating, the LED on the back panel of the RWA-2550++ is turned red.

13.3 ANA-971++ Power Troubleshooting

There are surge protectors in the ANA-971++. LED indicators display the current state of the machine: all green is OK, one or more off indicates ok but something is not right, and one or more red indicates a short circuit faulty line. In case of a short circuit, some (or all) power sources are disconnected from the ANA-971++, and the corresponding LED indicator(s), located near to the power inlet, are turned red.

There is protection for short circuits in the ANA-971++. In case of a short circuit on the Universal Preamplifier 7 board on +/- 5V, power to the Universal Preamplifier 7 board is disconnected and the WITE software issues an error message (UP power off).

To recover from this situation, recycle the power of the RWA-2550++. If there is no short circuit, power is returned to the ANA-971++. If the problem persists, there is a short circuit. The short circuit can be caused

by wrong connections outside the ANA-971++, or malfunctioning replaceable modules like filters, differentiators and/or chip adapters. Check that the ANA-971++ power cable is properly connected to the RWA-2550++ and the ANA-971++.

CHAPTER 14

SOFTWARE TROUBLESHOOTING

14.1 Error Messages

The structure of test system software is such that there are several parts performing different functions and interchanging with information:

- a user interface called WITE

NOTE: For WITE error messages, see the *WITE User's Guide* (Volume I of the WITE manual set).

- external modules (like W747 test)

NOTE: For external modules error messages, see the *WITE External Modules Guide* (Volume II of the WITE manual set).

- device drivers that unify interface to different spinstands, drives, etc

NOTE: For device driver error messages, see the corresponding manual for each particular device driver.

- the TST library
- the DLB library

Device drivers are different for different external devices, but not for different RWA models. In case of problems met by any of these parts of software, they produce error messages. Thus, there exist error messages from WITE, from external modules, from device drivers, from the TST library, and from the DLB library.

Here we shall provide a list and explanations about error messages from TST and DLB libraries.

14.1.1 TST Library Error Messages

The following is a table containing error messages that the TST Library can produce, with the explanation of possible reasons and solutions. If a message is not in this table, call Guzik Technical Support.

NOTE: Only messages that can be produced while working with RWA-2550++ model are listed in the table.

Error Number & Message Text	*Possible Causes*	*Solution*
1 - No context configured	Internal software error	Contact Guzik Technical Support
2 - No more data in current context	Internal software error	Contact Guzik Technical Support
3 - Incorrect context tag	Internal software error	Contact Guzik Technical Support
4 - Error in error recovery	Internal software error	Contact Guzik Technical Support
5 - ...:Base TAA equal 0.0	Very low level of signal is measured	Check head and head adapter connection
	Wrong overwrite filter settings, bad head, bad head amplifier	Check overwrite test setup
6 - ...:Base TAA not measured	In Overwrite, Resolution or SNR test the first measurement of TAA is missing	Re-initialize software, check that head(s) can read and write
7 - Number of active TAA samples is 0.0	There were no ADC samples within the Read Gate	Increase the Read Gate. If it doesn't help, contact Guzik Technical Support
8 - Amplitude count is 0.0 through filter ...	The signal level at peak detector is 0.0	Check R/W Data Cable connections
	Hardware problem	Check whether filter is installed
		Contact Guzik Technical Support
9 - Out of memory heap	Not enough heap memory	Contact Guzik Technical Support
10 - Signal level too low	Level of signal is very low	Check the read data connections. Be sure the head can read and write
11 - BSA: array overflow	Internal software error	Contact Guzik Technical Support
12 - ...: Cannot open file '...'	Pattern file '...' doesn't exist	Check pattern file name
	Cannot open file '...' for writing	
13 - BSA: Bit shift was not calibrated	Bit shift was not calibrated	Calibrate Bitshift
14 - BSA: Bitcell period ... out of range, min ... max ...	System period is out of range	Bitcell period should be within 4...200 ns for RWA-2550++
18 - Cannot load pattern	Cannot load pattern from .EPT file. Possibly, too many patterns (>40) are in one file	Remove unused patterns from the pattern file
		Split pattern file
27 - PAT: Pattern not loaded in pattern memory	Selected pattern is not in the pattern file currently used	Check pattern file name spelling and contents
33 - POP: Parameters larger than Sector/Index	Inconsistent set of popcorn parameters	Check popcorn test parameters: POPWRGLEN, POPRDGLEN, POPDELAY in GITE and Write Gate Length, Read Gate Length and Delay in WITE
34 - POP: Extra pulse errors found at test threshold	During popcorn test the extra pulses were found in nonpop-	Set the threshold higher to avoid counting noise as a popcorn

found at test threshold	corn mode	counting noise as a popcorn
35 - ... : Cannot use Overwrite Filter for this test	Measurement can not be done through the spectrum analyzer	Select one of the main filters (F0F3) for this test
37 - PW: Zero or not stable pulses count	Number of read data pulses is zero:	Check signal from the head
		Check cable connections
	R/W Data Cable not connected	Contact Guzik Technical Support
	Hardware problem	
38 - BSARATE: Low count of pulses	Number of read data pulses is very low:	Check signal from the head
		Check that differentiator is installed
	Differentiator not installed	
	R/W Data Cable not connected	Check cable connections
	Hardware problem	Contact Guzik Technical Support
39 - BSARATE: sample size ... invalid	Sampling level is not in the 3 to 10 range	Select sampling level in the range from 3 to 10
40 - BSARATE: window is not set	The Bit Cell window is not set	Specify the size of Bit Cell window
43 - PRECOMP: precomp not calibrated	Precompensation hardware is not calibrated	Calibrate precomp
44 - Illegal bit shift margin value	Internal software error	Contact Guzik Technical Support
45 - ... : RMS is too small	No signal in the ANA-971++ input	Check head cables, check signal in the Read Channel Output
48 - Memory heap is corrupt	Internal software error	Contact Guzik Technical Support
52 - DEVICE Base address is not found	Unable to detect RWA	Check Guzik Host Adapter board and Computer cable
53 - ERROR: RWA OFF	Power is off or Power Cable is damaged or not connected	Check Power Cable
	Computer Interface Cable is not connected	Check Computer Interface Cable
54 - ERROR: RWA WAS OFF	During the test power was off	Reinitialize RWA
55 - ERROR: LINEAR BOX IS OFF	Power is off in the ANA-971++	Check the AB Power Cable
		Check the R/W Control Cable
		Check breakers in the ANA-971++ and turn power off and then on again
56 - DEVICE is not SELECTED or not READY	Drive or spinstand became not ready	Check the device and cable connections
57 - PAT: not a valid pattern	No pattern is selected or software is not completely initialized	Select a pattern or reinitialize software
58 - PAT: cannot find ... pattern	Internal software error	Contact Guzik Technical Support
59 - Failed to set pop mode. Check parameters and sector	Popcorn test can not be performed in hard sector mode	Check sector mode and popcorn test parameters

mode.		
60 - Attempt to release bad pointer	Internal software error	Contact Guzik Technical Support
61 - Bad ... calibration table(s) size	Precomp or bit shift calibration table size mismatch in the RWA.CLB file Possibly corrupted file	Recalibrate RWA-2550++ and save calibration file
62 - PATFILE: Multiple definition of pattern ...	Two or more patterns with the same name are defined in the .EPT file	Each pattern in the .EPT file must have unique name
63 - PATFILE: Error during loading pattern ... , pattern deleted	Pattern can not be loaded from .EPT file because of the previous errors	Fix the problems that caused previous error messages
64 - PATFILE: Syntax error in line ... : ...	Syntax error in .EPT file or, possibly, the file has been corrupted	Recompile .PDL file to .EPT file using pattern compiler. If problem persists contact Guzik Technical Support
65 - PATFILE: Palette index out of range ...	Inconsistent .EPT file or, possibly, the file has been corrupted	Recompile .PDL file to .EPT file using pattern compiler. If problem persists contact Guzik Technical Support
66 - ERROR: ANALOG BOX WAS OFF	ANA-971++ was off during the test	Reinitialize the system
67 - Calibration file is from different RWA. It is ignored.	Wrong calibration file	Recalibrate RWA-2550++ and save calibration file
69 - PRML: Address Marker not found	Address Mark not found in PRML signal	Check the signal and pattern
70 - COFF: Cannot open file, or bad file type ...	Software installation files are corrupted Incomplete software installation	Reinstall software
71 - COFF: ... not an IPL program.	Bad or corrupted file Incomplete software installation	Try to reinstall software If problem persists, contact Guzik Technical Support
72 - COFF: Error reading ….	Bad or corrupted file Incomplete software installation	Try to reinstall software If problem persists, contact Guzik Technical Support
81 - SCAN: Unknown scanning mode (...)	Internal software error	Contact Guzik Technical Support
82 - SCAN: Must have two heads only	5, 6 or 8revolution mode is selected, but number of heads is not equal 2	Select HDA mode for number of heads equal 2
83 - SCAN: At least one head must be selected	No head is selected in the system for testing	Select head(s)
84 - SCAN: Must not be in sector	5, 6 or 8revolution mode can	Use HDA mode without sectors

mode	not run in sector mode	for scanning test
85 - SCAN: Wait for seek completed time out	It takes too long for a device (a drive or a spinstand) to finish seek to next track	Possibly, device hardware problem Contact Guzik Technical Support
86 - SCAN: Undefined test head number (...)	Internal software error	Contact Guzik Technical Support
87 - SCAN: Unsupported HDA scan rev (...)	Internal software error	Contact Guzik Technical Support
88 - SCAN: Cannot skip revolution after writing	5, 6 or 8revolution mode can not skip a revolution after writing	Disable “Skip Revolution after writing” or Use HDA with this option
91 - SCAN: Cannot do read-only test with 5 rev mode	5revolution mode doesn’t support readonly test	Select some other modes or Enable read/write operations for 5rev. mode
93 - TRK_PROF: Device does not support offset operations	A device (a drive or a spinstand) does not have offset operations required for track profile test	You can not run track profile test with a device that does not have offset operations
94 - TRK_PROF: Cannot perform Track Profile: Invalid micro step size ...	Micro step size returned by a device is invalid (not positive)	Possible software error in a device driver implementation. Contact the device manufacturer
95 - TRK_PROF: The ‘FROM’ parameter exceeds the maximum offset ...	Track profile test parameter exceeds the device capabilities	Change parameter to a reasonable for this device value
96 - TRK_PROF: The ‘IN’ parameter exceeds the maximum offset ...	Track profile test parameter exceeds the device capabilities	Change parameter to a reasonable for this device value
97 - TRK_PROF: Cannot perform Track Profile: Invalid number of steps ...	Track profile test ‘number of steps’ parameter is invalid (not positive). This is Internal error	Contact Guzik Technical Support
100 - Too few sectors per revolution. Min(Sectors)=...	Internal software error	Contact Guzik Technical Support
101 - Too many sectors per revolution. Max(Sectors)=...	Internal software error	Contact Guzik Technical Support
102 - VFO board isn't installed: cannot execute ... in Peak-Detection-mode	The specified test can not run in peak detection mode when there is no bit shift analyzer installed	You can not run peak detection mode tests without bit shift analyzer

Table 16 TST Library Error Messages

14.1.2 DLB Library Error Messages

The DLB Library error messages are grouped into four categories according to their severity. There are fatal errors, warning errors of two levels of severity and internal errors. The following is the definition of all these categories.

Error Message Type	*Definition*
DLB Fatal errors	These are hardware errors that prevent the RWA-2550++ from continuing an operation. In some cases, the software may need to be re-initialized. All fatal error messages are numbered between 0 and 999.
DLB Warning Level 1	These are hardware errors that are caused by starting an operation but usually allow the operation to continue. All level 1 warnings are numbered between 1000 and 1999.
DLB Warning Level 2	Similar to warning Level 1 but are generally less critical errors. All level 2 warnings are numbered between 2000 and 2999.
DLB Internal errors	Software/Hardware related errors that are not generally observed by the user. All internal errors are numbered between 20000 and 24999.

Table 17 DLB Library Error Types

NOTE: If you see any error or warning messages that are numbered between 0 and 24999 but not listed, contact Guzik Technical Support.

14.1.2.1 DLB Fatal Errors

NOTE: Only messages that can be produced while working with RWA-2550++ model are listed in the table.

Error Number & Message Text	*Possible Causes*	*Solution*
2 - Wait for index time out	Caused when the software detects absence of index. Cause could be: Malfunctioning drive/spinstand Missing device control cable connection.	Replace drive/spinstand with another one. Check again. Check device control cable connection.
3 - No read index	Missing index causes hardware flag to be set. Same cause as for error 2.	Refer to error 2.
4 - RWA offline	Power switch is OFF Missing power cable connection Missing RWA-2550++ computer cable connection Guzik Host Adapter board has wrong base address Guzik Host Adapter board is broken Other hardware in computer conflicting with Guzik Head Adapter board address.	Check power LED in front. If off, check switch Check power cable. If on, check computer cable. Check Guzik Head Adapter board base address. Replace with another adapter board Remove all other installed boards from the computer and try again.
5 - Analog box offline	Power Switch is off Missing ANA-971++ power connection ANA-971++ circuit breakers tripped. Missing R/W Control cable connection	Check LED on back of ANA-971++. If off, check switch Check power connection with RWA-2550++ Check circuit breakers in ANA-971++. Check R/W control cable.
8 - RWA power interrupted	Usually happens if RWA-2550++ power is switched Off and then On again, without reinitializing the software. Also refer to error 4.	Reinitialize software. Check Guzik Head Adapter board, base address, or other installed hardware in computer (refer to error 4)
9 - Device offline	Missing drive control cable Drive/spinstand power off or malfunction.	Check if the drive control cable is connected. Check that the drive or spin/stand power is on.
10 - Unit not ready	RWA-2550++ or ANA-971++ is offline.	Refer to errors 4 and 5.

11 - Reference oscillator broken - #	RWA-2550++ internal hardware problem	Reboot system and check again. If problem persists, contact Guzik Technical Support. Note the # indicates some displayed number. Write down this number.
12 - VFO lost sync	RWA-2550++ internal hardware problem	Reboot system and check again. Verify scope points; when not in read mode the 2FVFO frequency should be twice the 1FPLO frequency. In read mode, VFO should be locked to data. If problem persists, contact Guzik Technical Support.
13 - PLO fails, 2F period - #	If it happens in "scanning" mode this should be followed by another message about external clock. In that case, it could be a failure of external clock enable, or the servo clock from the drive or a wrong servo clock frequency. If not in "scanning" mode it could be caused by RWA-2550++ internal hardware failure.	Verify on the scope point that PLO is the same as the bit cell frequency set in software. Reboot system if RWA-2550++ hardware failure is suspected. If problem persists, contact Guzik Technical Support. Note: the # indicates some displayed number. Write down this number. Check if the jumper setting of the host adapter card is in conflict with the I/O address used by the computer resources.
23 - Analog box power interrupted	Usually happens if ANA-971++ power is switched Off and then On again, without reinitializing the software.	Reinitialize software.
24 - Universal Preamp power off	UP revision 6 or higher: power is off	Check the ribbon cable from ANA-971++ to the UP. Reinitialize software
25 - Universal Preamp power interrupted	UP revision 6 or higher: power temporarily was off the UP	Check the ribbon cable from ANA-971++ to the UP. Reinitialize software
28 - Missing/Bad license number	The license for software doesn't match RWA-2550++ serial number	Contact Guzik Technical Support
32 - API Error '...' - ...	Internal software problem	Contact Guzik Technical Support
39 - Spectrum Analyzer: EEPROM/hardware incompatibility detected	Wrong hardware configuration has been detected. Should not ever occur	Contact Guzik Technical Support
40 - Read Gate Limits do not comply 0% <= ...(start) <= ...(stop) <=100%	Read gate boundaries are out of their limit.	Set Read gate to some reasonable values. If the problem persists, contact Guzik Technical Support

41 - Altera error: ...	Can be hardware problem or problem with opening some files	Check, whether software is properly installed. Contact Guzik Technical Support
42 - PLO: External PLL not locked	Hardware problem Wrong frequency of the external clock is specified in software	Contact Guzik Technical Support Check external clock frequency
43 - PLO: Internal PLL not locked	Hardware problem	Contact Guzik Technical Support
44 - PLO: Serialyzer always busy	Should not ever occur. Hardware problem	Contact Guzik Technical Support
45 - ERAI - board should be [FabP/N]=... [Ass]=... and higher in RWA w/o VFO - board	Wrong hardware configuration	Contact Guzik Technical Support
46 - Envelope memory board is not detected	Hardware problem	Contact Guzik Technical Support
47 - Latch result on index in SDP board timeout	This means malfunctioning of hardware	Contact Guzik Technical Support
48 - Failed to recover Envelope Memory, please restart program	Most likely, it is a hardware problem	Try to restart software. If the problem persists, contact Guzik Technical Support
49 - Incompatible RWA and AB revisions. READ CHANNEL CANNOT BE COMPLETED!	Wrong hardware configuration. Should not ever occur	Contact Guzik Technical Support

NOTE: All fatal error messages are numbered between 0 and 999. If you observe any warning messages with numbers between these limits that are not listed below, contact Guzik Technical Support.

Table 18 DLB Fatal Errors

14.1.2.2 DLB Warnings, Level 1

NOTE: Only messages that can be produced while working with RWA-2550++ model are listed in the table.

Error Number & Message Text	Possible Causes	Solution
1001 - Illegal count source translation - #	Internal Software Problem.	Contact Guzik Technical Support
1002 - Illegal write data selection - #	Internal Software problem.	Contact Guzik Technical Support
1003 - Address mark not found	No read signal	Check scope point for analog read signal
	Read signal present but read channel setup incorrect for that data rate.	Check if filter and differentiator selected are correct for current data rate
	RWA-2550++ internal hardware failure.	Reboot system and check again. If problem persists, contact Guzik Technical Support.
1006 - Cannot prescale external clock	External clock frequency is out of range 1 MHz – 1310 MHz	Check external clock frequency and its setting in software
	Hardware problem	Contact Guzik Technical Support
1007 - Deselect external clock error	Can happen only in scanning mode	Check presence of external clock
	External servo clock failure	Ensure that the correct value of clock frequency is set
	External clock frequency does not match value specified.	Using scope points check that 2FVFO is twice the frequency of 1FPLO
	RWA-2550++ internal hardware failure	Reboot system and check again. If problem persists, contact Guzik Technical Support
1008 - Select external clock error	Same as warning 1007	Refer to warning 1007
1010 - Clock settling time too long	Internal software problem	Reboot system and check again. If problem persists, contact Guzik Technical Support
	RWA-2550++ internal hardware problem	
1011 - Read gate boundary error - ##	Illogical read gate setting	Check if read gate setting is reasonable, for example read gate start<end
	Bad data files or software problem	Contact Guzik Technical Support
1013 - Write gate boundary error, nsec - ##	Illogical write gate setting	Check if write gate setting is correct, for example write gate beginning<end
	Bad data files or software problem	Contact Guzik Technical Support

1014 - Write gate boundary error, byte - # #	Illogical write gate setting Bad data files or software problem	Check if write gate setting is correct, for example write gate beginning<end Contact Guzik Technical Support
1015 - Bit shift calibration samples low - #	This may happen only during bit shift calibration. RWA-2550++ internal hardware problem	Reboot system and check again. If problem persists, contact Guzik Technical Support.
1016 - No VFO error(#) - #	This may happen only during bit shift calibration. RWA-2550++ internal hardware problem	Reboot system and check again. If problem persists, contact Guzik Technical Support.
1019 - Illegal scope sync sector - #	No of sectors is less than sync sector specified Bad data files or software problem	Check number of sectors and sync sector specified Contact Guzik Technical Support
1021 - Main gain signal saturated	Signal level is too high RWA-2550++ internal hardware problem	Check signal level Reboot system and check again. If problem persists, contact Guzik Technical Support.
1022 - Overwrite gain signal saturated	Signal level is too high measured through the spectrum analyzer RWA-2550++ internal hardware problem	Check signal level Reboot system and check again. If the problem persists, contact Guzik Technical Support
1024 - EEPROM read cycle checking error	RWA-2550++ internal hardware problem	Reboot system and check again. If the problem persists, contact Guzik Technical Support.
1026 - Scope point 3 conversion error - #	Internal software problem	Contact Guzik Technical Support
1027 - Scope point # illegal source - #	Internal software problem	Contact Guzik Technical Support
1028 - X24022 EEPROM no acknowledge	ANA-971++ or UP7 internal hardware problem	Reboot system and check again. If the problem persists, contact Guzik Technical Support.
1029 - X24022 EEPROM wait for write finish time out	ANA-971++ or UP7internal hardware problem	Reboot system and check again. If the problem persists, contact Guzik Technical Support.
1030 - X24022 EEPROM wrong write page size - #	Internal software problem	Reboot system and check again. If the problem persists, contact Guzik Technical Support.
1031 - # revolution mode: number out of range - #	Internal software problem	Contact Guzik Technical Support.

1032 - Invalid EEPROM parameter value	VFO EEPROM data is possibly corrupted	Reboot system and check again. If the problem persists, contact Guzik Technical Support.
1033 - Invalid CRC in ... EEPROM	EEPROM data is possibly corrupted	Reboot system and check again. If the problem persists, contact Guzik Technical Support.
1034 - ... EEPROM read error	Invalid data was read from the Filter EEPROM	Reboot system and check again. If the problem persists, try to replace the specified filter. Contact Guzik Technical Support.
1035 - EEPROM I2C bus error	Hardware problem is detected while accessing one of the EEPROMs	Contact Guzik Technical Support
1040 - PG: Wrong write data source selection	Illegal parameter value in product files	Resave the product configuration
	Internal software problem	Contact Guzik Technical support
1041 - Incompatible UP configuration: ... - ...	Software did not recognize the UP7 configuration	Contact Guzik Technical Support
1042 - Invalid ... Interface board revision:	Software did not recognize the HA Interface board.	Contact Guzik Technical Support
1044 - No Head Amplifiers connected	Software did not find any Head Amplifiers connected to UP7	Check ribbon cables between Interface board and Head Amplifiers
1045 - PFR: Cut - off frequency - #, out of range	The cutoff frequency cannot be set for programmable filter	Change filter type or frequency, resave configuration
1046 - PFR: Boost factor - #, out of range	The boost factor cannot be set for programmable filter	Change filter type or boost factor, resave configuration
1047 - CAD: Chip ... does not match the EEPROM: ...	Chip type stored in the EEPROM doesn't match the settings in the data file	Make sure the correct chip type is specified in the setup. If correct chip type was selected, contact Guzik Technical Support
1049 - HF VFO supports 1 or 3 zeros preambles only	RWA-2550++ bit shift analyzer supports patterns with preambles having either 1 or 3 zeroes between ones	Use a proper pattern in peak detection mode
1050 - Spectrum Analyzer frequency ... is out of range	The attempt to used frequency for the spectrum analyzer that is out of it operational range	Check setup for the test causing this problem
1051 - Unable to calibrate Spectrum Analyzer: main attenuator is not calibrated	This is a secondary message you get after main attenuator calibration has failed. The latter can occur if there are no filters installed in the read channel	Check ANA-971++ configuration. If the problem persists, contact Guzik Technical support

1052 - CAD: cannot load DLL ...	Software did not find a required file for the chip installed. Probably, incomplete or wrong software installation.	Install new software Contact Guzik Technical support
1054 - CAD: chip type ... not supported	The installed chip is not supported by this version of software	Install new version of software Contact Guzik Technical support
1056 - Analog Box DSP Timeout: ...	Some problem has occurred in communication with the ANA-971++	Check connections Contact Guzik Technical support
1057 - HA interface is not compatible with removable HA, use Universal Interface Rev. J1 or K1	Current UP7 configuration is incompatible	Use compatible Head Amplifiers and Interface boards Contact Guzik Technical support
1058 - Analog Box DSP Buffer Overflow	Internal software problem	Contact Guzik Technical support
1059 - Address Mark length should be 1..8 bits in Chip Adapter mode	Pattern is inconsistent with current configuration: wrong AM is used	Use proper patterns in chip adapter mode
1060 - Chip Adapter parallel data width should be 1,2,4,8 bit(s)	Internal software problem	Contact Guzik Technical support
1061 - UP gain signal saturated	Dynamic range of the UP7 attenuator is not enough to bring the input signal to the nominal level. Can be hardware problem	Check signal level from the Head Amplifier. Contact Guzik Technical support
1065 - No filter in the slot #0. Calibration is not possible	No filter is installed into the slot #0 or the filter installed is broken	Check filter in the slot #0 and restart software. If the problem persists, contact Guzik Technical support

NOTE: All level 1 warnings are numbered between 1000 and 1999. If you observe any warning messages with numbers between these limits that are not listed below, contact Guzik Technical Support.

Table 19 DLB Warnings - Level One

14.1.2.3 DLB Warnings, Level 2

NOTE: Only messages that can be produced while working with RWA-2550++ model are listed in the table.

Error Number & Message Text	Possible Causes	Solution
2002 - Low env samples - #	Software internal problem RWA-2550++ internal hardware problem	Reboot system and check again. If the problem persists, contact Guzik Technical Support.
2004 - Index checking RPM too low	Attempt to set RPM to value below minimum (about 40)	Increase RPM and recheck
	Index missing: control cable not connected or device malfunction	Check device control cable connection
2014 - System period out of bound	An attempt to set frequency too high or too low	Set system frequency to correct value and save the setup
2015 - System period ... > allowed ... for BS calibration	Frequency is too low for bit shift calibration and measurements	Set higher frequency
2016 - Operation interrupted by user	User hit a key during a measurement or a calibration (some measurements will detect this event and abort execution)	Restart operation if desired
2017 - Unknown programmable filter ...	Hardware problem with the filter installed	Check filter installation
	Software did not recognize programmable filter	Contact Guzik Technical Support for software upgrade.
2018 - Unknown sector type - ...	Internal software problem	Contact Guzik Technical Support
2019 - Out of application pattern handles	Too many patterns specified by user	Reduce number of patterns and retry
	Internal software error	Contact Guzik Technical Support
2020 - Out of pattern memory	Too big patterns	Reduce patterns size
	Internal software problem	Contact Guzik Technical Support
2021 - Out of application bit mask handles	Internal software error	Contact Guzik Technical Support
2023 - Out of application preamble handles	Internal software error	Contact Guzik Technical Support
2024 - Out of preamble memory	Patterns used are too complicated	Use more simple patterns
	Internal software error	Contact Guzik Technical Support
2030 - Out of reserved precomp handles	Internal software error	Contact Guzik Technical Support

2032 - Byte aligned pattern too long - #	User specified pattern is too irregular and too long (cannot be aligned to byte boundaries)	Reduce pattern length or make it more regular
2034 - Signal unstable during main gain adjustment	The external signal is unstable	Check external signal and try again
2035 - Signal unstable during overwrite gain adjustment	Same as error 2034	Refer to error 2034
2036 - Low samples for threshold 100 calibration - #	RWA-2550++ hardware problem	Reboot system and try again. If problem persists contact Guzik Technical Support
2037 - Signal unstable during threshold 100 calibration	Same as error 2034	Refer to error 2034
2038 - Special write frequency is out of range	Attempt to write too high flux frequency	Choose lower frequency
2039 - Index inside counting gate - #	Read gate is too long	Reduce read gate length and retry
	Index jitter is too big (index occurs inside read gate)	
	Read clock unstable	Check the read signal
2040 - Precomp calibration failed - #	Corrupted data file	Recalibrate precomp and try again
	RWA-2550++ internal hardware problem	Reboot system and try again. If the problem persist, contact Guzik Technical Support
2041 - Out of pattern control memory	Pattern is too complicated	Simplify pattern and retry
	Software internal problem	Contact Guzik Technical Support
2042 - Inconsistent pattern handle	Internal software error	Contact Guzik Technical Support
2043 - Inconsistent bit mask handle	Internal software error	Contact Guzik Technical Support
2044 - Inconsistent preamble handle	Internal software error	Contact Guzik Technical Support
2045 - Inconsistent precomp handle	Internal software error	Contact Guzik Technical Support
2047 - BSC closed window calibration failed	RWA-2550++ internal hardware problem	Reboot system and try again. If the problem persists, contact Guzik Technical Support
2048 - BSC centering failed - #	RWA-2550++ internal hardware problem	Reboot system and try again. If the problem persists, contact Guzik Technical Support
2049 - Out of control Memory handle	Internal software error	Contact Guzik Technical Support
2050 - Control program generation failed on pgm #...	Internal software error	Contact Guzik Technical Support
2051 - Out of MTBS memory	Internal software error	Contact Guzik Technical Support
2052 - Out of BTBS memory	Internal software error	Contact Guzik Technical Support

2053 - Unknown write gate selection	Internal software error	Contact Guzik Technical Support
2054 - BSC delay line measurement failed	RWA-2550++ internal hardware problem	Reboot system and try again. If the problem persists, contact Guzik Technical Support
2055 - TAA out of range during attenuator calibration - #	Bad connection between RWA-2550++ and ANA-971++	Check all connections.
	One of the filters is not installed.	Check all filters.
	Hardware problem in the ANA-971++	Select Read Data on Scope point on back panel of RWA-2550++ and check the read signal on scope.
2056 - Can not set gain - attenuator is not calibrated	This is a secondary message after attenuator calibration has failed	Fix the problem with attenuator calibration and restart software
2057 - Can not select nop pattern (...)	Internal software error	Contact Guzik Technical Support
2060 - Timing relation too complex for control program, space required - ...	Internal software error	Contact Guzik Technical Support
2061 - Chip data rate out of range - ...	Frequency is too high for the chip installed	Select lower frequency
2062 - Calibration table is non monotonic	Hardware problem	Reboot system and try again. If the problem persists, contact Guzik Technical Support
2064 - EPTN - out of pattern memory	Patterns do not fit into memory	Make patterns smaller
2069 - Spectrum Analyzer: TAA out of range after Main Gain adjustment: ...	Input analog signal is too high and saturates main attenuator	Check input signal
	Internal software problem	Call Guzik Technical support
	Hardware problem	
2070 - Spectrum Analyzer: Failed to adjust 0 dB level. Last TAA - ...	Internal software or hardware problem	Try to restart software. If the problem persists, call Guzik Technical support
2071 - Spectrum Analyzer: Internal error #1 while calibration	Internal software or hardware problem	Try to restart software. If the problem persists, call Guzik Technical support
2072 - Spectrum Analyzer: Failed to calibrate ... dB level	Internal software or hardware problem	Try to restart software. If the problem persists, call Guzik Technical support
2073 - Spectrum Analyzer: Attenuator is not calibrated	This is a secondary message, caused by spectrum analyzer attenuator calibration failure	Fix the original problem. Try to restart software. If the problem persists, call Guzik Technical support

2075 - Can't measure MR impedance: no Read BIAS	Currently set bias current is zero. Either wrong configuration or user mistake	Check configuration and set non-zero bias current
2076 - Spectrum Analyzer: PLL ... is not locked after initialization	Internal software or hardware problem	Try to restart software. If the problem persists, call Guzik Technical support
2078 - Spectrum Analyzer: TAA always zero during 0 dB calibration	Internal software or hardware problem	Try to restart software. If the problem persists, call Guzik Technical support
2079 - VFO board doesn't exist in current hardware configuration. Operation can't be performed - ...	Bit shift analyzer is not installed or has not been detected in this RWA, that's why the displayed operation could not been performed	If Shift Analyzer has not been detected, try to restart software. If the problem persists, call Guzik Technical support
2080 - Signal unstable during up gain adjustment	Unstable signal was detected during adjustment of gain on the UP7	Check the signal and repeat the procedure
2081 - Failed to retrieve results on Read Gate	Either hardware or software internal problem	Try to restart software. If the problem persists, call Guzik Technical support
2082 - TAA = ...; too far from expected value: ...	Internal software or hardware problem during main attenuator calibration	Try to restart software. If the problem persists, call Guzik Technical support
2083 - Attn DAC is saturated: ...; while TAA = ... on ... samples, due level not reached	Internal software or hardware problem during main attenuator calibration	Try to restart software. If the problem persists, call Guzik Technical support
2084 - Precomp failed - ...; G=...; N=...; T=...; C=...; Z=...	Internal software or hardware problem during calibration of precomp	Try to restart software. If the problem persists, call Guzik Technical support
2086 - Zero Delay failed: C#...	Internal software or hardware problem during calibration of precomp	Try to restart software. If the problem persists, call Guzik Technical support

NOTE: All level 2 warnings are numbered between 2000 and 2999. If you observe any warning messages with numbers between these limits that are not listed below, contact Guzik Technical Support.

Table 20 DLB Warnings - Level Two

14.1.2.4 DLB Internal Errors

NOTE: Only messages that can be produced while working with RWA-2550++ model are listed in the table.

Error Number & Message Text	Possible Causes	Solution
20000 - Non - implemented function called	Internal software error	Contact Guzik Technical Support
20001 - Non available function called	Internal software error	Contact Guzik Technical Support
20002 - Unknown error code - ...	Internal software error	Contact Guzik Technical Support
20003 - Unknown clock failure code - ...	Internal software error	Contact Guzik Technical Support
20004 - Unknown read gate mode - ...	Internal software error	Contact Guzik Technical Support
20006 - Unknown write gate mode - ...	Internal software error	Contact Guzik Technical Support
20007 - Unknown gate control mode - ...	Internal software error	Contact Guzik Technical Support
20008 - Unknown system status code - ...	Internal software error	Contact Guzik Technical Support
20011 - Unknown scan source code - ...	Invalid data source for comparator is selected	User software error in a custom external module
	Internal software error	Contact Guzik Technical Support
20013 - Cannot find precomp delay	RWA-2550++ internal hardware problem	Restart system, recalibrate precomp and try again. If the problem persists contact Guzik Technical Support
20015 - Error file look ahead buffer overflow	Internal software error	Restart system and try again. If the problem persists contact Guzik Technical Support
20016 - Error file inconsistent tag - ...	Internal hardware or software problem	Restart system and try again. If the problem persists contact Guzik Technical Support
20017 - Pattern control memory value out of range - ...	Internal software error	Try to restart software. If the problem persists, call Guzik Technical support
20018 - Pattern memory allocation list corrupted	Internal software error	Try to restart software. If the problem persists, call Guzik Technical support
20019 - BSC can not select parameters (prd=..., bs=...)	Internal hardware or software problem while bit shift analyzer calibration	Try to restart software. If the problem persists, call Guzik Technical support

20020-Bad control memory handle	Internal software error	Try to restart software. If the problem persists, call Guzik Technical support
20022-MTBS program too big - ...	Internal software error	Try to restart software. If the problem persists, call Guzik Technical support
20024-No device driver program for head inquire	Device (spinstand or drive) driver software problem. The program to inquire number of heads from the driver is not implemented	Fix device driver problem
20025-Bad cluster port table: ...	Internal structures of software data are corrupted. Can be caused by customer external module software bugs	Debug external customer module, if one is used. Contact Guzik Technical Support
20028-Analog Box DSP: wrong length in function ...	Internal software error	Try to restart software. If the problem persists, call Guzik Technical support
20029-PLO: Clock source undefined	Internal software error	Try to restart software. If the problem persists, call Guzik Technical support

NOTE: All internal errors are numbered between 20000 and 24999. If you observe any messages with numbers between these limits, which are not listed below, contact Guzik Technical Support.

Table 21 DLB Internal Errors

APPENDIX A

DATA RATE TERMINOLOGY

A.1. Data Frequency Terms in Graphic Format

Figure 17 illustrates the data rate terminology terms graphically.

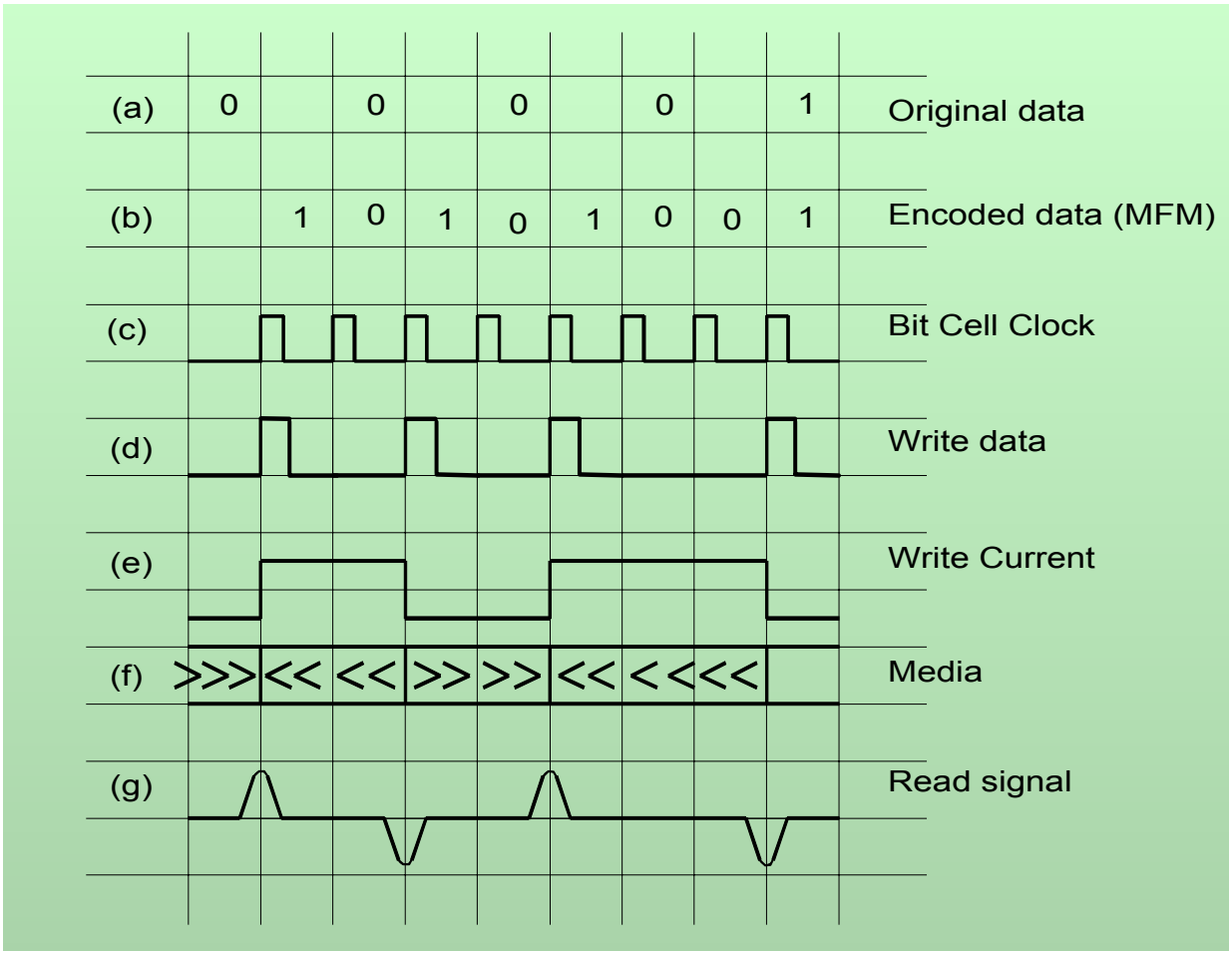


Figure 17 Terms and Data Rates

A.2. Data Frequency Terms Definitions

There are several specific terms related to data frequency in magnetic recording area. Below is the term definitions used in all Guzik Technical Enterprises documentation and software.

Term	*Definition*
Original Data	Digital binary data to be stored. This data is input/output from/to a storage device.
Encoded Data	data obtained from the original by encoding. To achieve better performance of a storage device, the original data is being encoded. This process is reversible, such that the original data can be restored from the encoded one. Different recording methods require different data encoding. Peak detection method usually uses MFM, 1-7 and 2-7 encoding schemes, while PRML applies 8/9 in most cases. As a rule, number of bits after encoding increases and one of the characteristics of an encoding scheme is a ratio between original number of bits and number of bits after encoding. For MFM it is 1:2, for 1-7 it is 2:3, for 2-7 it is 3:4 and for 8/9 it is 8:9. For more details on different encoding schemes see WITE software manual.
Bit Cell Clock	Clock write channel is working with. There is a clock pulse per each encoded bit.
Write Data	Sequence of pulses derived from the Bit Cell Clock, where there is a pulse at each clock that is corresponding to one in the encoded data and there are no pulses at the clocks corresponding to zeroes.
Write Current	Current through the write element of the head, i.e. inductive coil. Write current toggles its direction at each Write Data pulse.
Direction of Magnetization on a Media	A head magnetizes media surface either in one direction or in another, depending upon in which direction write current flows through the head. Magnetization changes direction in places where the Write Data pulses occur.
Flux Reversal	A place where magnetization of the surface changes its direction.
Read Signal	Analog signal produced by a read element of a head. It consists of positive and negative pulses at the places of Flux Reversals. Polarity of the pulses depends upon from which direction to which magnetization of the surface changes. Adjacent pulses always have different polarity.

Table 22 Data Frequency Term Definitions

NOTE: Other sources may assume different meaning for the same words.

A.3. Data Rate Terms

In correspondence with these definitions several terms regarding data rate (or data frequency) can be defined as follows.

Term	*Definition*
Encoded Data Rate	frequency of the Bit Cell Clock.
Decoded Data Rate	Bit Cell Frequency multiplied by encoding scheme ratio.
Flux Frequency	a frequency that corresponds to the minimal period between adjacent flux reversals. It depends upon Bit Cell Frequency and encoding scheme. For MFM and 1-7 it is a half of the bit cell frequency for 2-7 it is 1/3 of the bit cell frequency and for 8/9 it is equal to the bit cell frequency
Analog Read Signal Frequency	A frequency which is twice less than the Flux Frequency.

Table 23 Data Rate Terminology Definitions

APPENDIX B

STATISTICAL FUNCTIONS DEFINITION

B.1. Statistical Functions

Let $\boldsymbol{X}$ be a random value and $\{X_i\}$ its observations in N cases, $i = 1,2,...N$.

We can define average value (mathematical estimation) for $\boldsymbol{X}$ as

$$\overline{\boldsymbol{X}} = \mathbf{M}\boldsymbol{X} = \frac{\sum_{i=1}^{N} X_i}{N} \qquad (1)$$

Standard deviation (dispersion) of the random value $\boldsymbol{X}$ is defined as

$$\sigma_X = \sqrt{\frac{\sum_{i=1}^{N} [X_i]^2 - N \cdot \overline{\boldsymbol{X}}^2}{N-1}} \qquad (2)$$

And, finally, stability of the random value $\boldsymbol{X}$ is defined as

$$COV_X = \frac{\sigma_X}{\overline{\boldsymbol{X}}} \qquad (3)$$

Error rate by definition is $R = \frac{E}{S}$, where E is number of bits in error and S is total number of bits.

For error rate $\{R_i\}$ measured in N iterations, we can define average, standard deviation and stability applying formulae (1) - (3):

$$\overline{R} = \frac{\sum_{i=1}^{N} R_i}{N}$$

$$\sigma_R = \sqrt{\frac{\sum_{i=1}^{N} R_i^{\,2} - N \cdot \overline{R}^{\,2}}{N-1}}$$

$$COV_R = \frac{\sigma_R}{\overline{R}}$$

Rather often error rate is expressed in logarithmic scale: $LR = -\log \overline{R}$.

APPENDIX C

TECHNICAL NOTES

C.1. Track Format of the RWA

Figure 18 shows track format of the RWA-2550++. The index is followed by 3 µs of zeroes (erased dead zone) at the start. Usually 40 µs (20 µs for sector mode) of special pattern, the **preamble**, is used to synchronize the PLL in the RWA-2550++ data recovery circuits (bit shift analyzer or PRML chip). At the end of the preamble, there is an **address mark (AM)**, which is a delimiter between the preamble and that data. The address mark is followed by the data pattern.

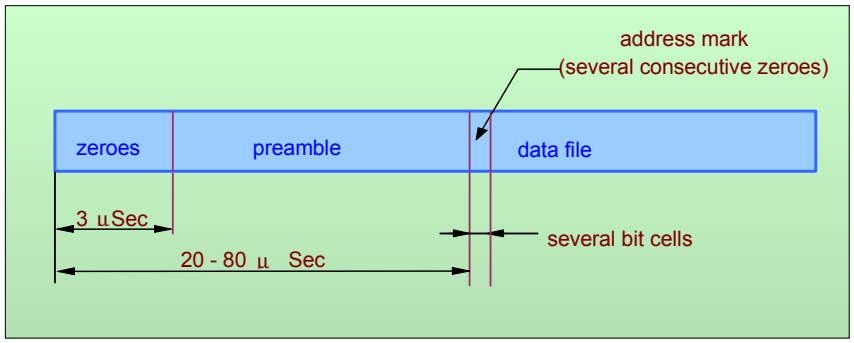


Figure 18 RWA Track Alignment

The preamble pattern and the length, number of zeroes in the AM and data pattern encoding depend upon the RWA-2550++ mode used (peak detection, chip adapter, Guzik PRML channel).

NOTE: The AM for the peak detector channel has several consecutive zeros.

NOTE: The AM for the PRML channel is dependent upon the particular channel used.

C.2. Peak Detector Time Constant and Charge Modes

The peak detector in the RWA-2550++ includes a RC discharge circuit. The capacitor is fixed and the resistor is variable and has 256 switched values. The capacitor is charged at the speed ≈1 mV/ns (or 4 mV/ns in Quick Charge mode). The discharge curve is $V(t) = V_0 \cdot \exp(-t/\tau)$, where t is time and τ is the time constant selected in software. The discharge curve can be approximated by linear function as $V = V_0\left(1 - t/\tau\right)$. 256 time constant settings are available from 1.5 to 384 µs; the setting specified by the user is rounded up or down to the nearest available one.

If the peak detector discharges 1% between signal peaks, the output of the detector follows the signal envelope rather close. A recommended time constant is 100·P, where P is the average time between flux transitions

Small changes in time constant have no significant effect on the detected signal envelope. A single time constant, e.g., 12µs (the default value) can be used in the range 2 to 10 MFlux/s with high accuracy. User has to be careful here: the signal frequency (determined by the number of transitions/s) depends on both the cell period and the distribution of ones and zeroes in the pattern. For example, a cell period of 100 ns and an 8000 pattern give a flux rate of 0.625 MFlux/s.

If the time constant is too small, e.g., 5µs for 1.5 MFlux/s, the detected envelope amplitude will be too low. This will cause TAA to be too small and PW measurements too high, since the threshold for PW is derived from the peak detector output voltage. If the time constant is high, e.g., 50µs for 10 MFlux/s, the output of the peak detector will not follow the signal modulation. Instead, the largest signal peaks will dominate the detected envelope. It is generally more safe to use a time constant larger than the one that has been calculated for the transition frequency in use.

The charge mode in the RWA-2550++ peak detector can be set to Quick or Slow. Unless the user explicitly specifies the charge mode, the slow charge mode is used for data frequencies below 50 MFlux/s, and the quick charge is used for the frequencies beyond this limit. Slow mode is compatible with old RWA-2550++ models and is recommended for signals with large PW (more than 40 ns), while the quick mode is working better with narrow pulses. If the slow charge mode is used for pulses with very small PW (e.g., 10 ns), the peak detector does not have enough time to charge the envelope to the peak of the signal. This will cause the envelope to be significantly lower than the peaks. If the quick charge mode is used for very wide pulses (e.g. 200 ns), the very fast charge of the peak detector can cause overshoots, thus distorting the envelope. It is usually more safe to use automatic selection of the charge mode, unless a very special measurement is being performed. For example, an attempt to use head/media combination with PW of 10 ns at data rate of 10 MFlux/s will require to switch the Quick Charge mode on.

C.2.1. Measurements Affected

Pulse Width (PW) is the measurement most sensitive to time constant and charge mode settings. If the time constant is too small, the PW measured is significantly higher than the actual value. For the PW measurement, time constant is automatically adjusted (see below).

TAA and modulation, signal-to-noise and RMS. The influence is obvious.

Overwrite test. The time constant must be correct for the frequency of the overwritten (usually LF) signal.

Resolution test. Generally speaking, the time constant should be set separately for HF and LF, but in a real HDA, there is only one time constant, the one suitable for HF. Set the time constant suitable for HF of the resolution tests.

Frequency test (refer to WITE software manual). This procedure runs various parametric tests over a range of clock frequencies; the time constant is automatically adjusted according to the current frequency (see below).

Calibration of TAA and Peak Detector. Time constant must be properly adjusted to the signal frequency used for calibration. Calibration signal frequency also must be selected properly based upon the estimated data rates for this set-up. Otherwise, all the subsequent measurements will be wrong.

C.2.2. Adjustment of the Time Constant

The basic time constant τ_0 is specified by user in software. This constant is used for all tests except of Frequency test and PW measurement.

In the **Frequency test**, the clock frequency is changes from the initial F_0 to higher frequencies with some step. At every stage of the test where current frequency is F_c, time constant is set to $\tau = \tau_0 \cdot F_0 / F_c$.

In the **PW test**, the average time between peaks (P) is determined and the time constant is automatically set to 100·P.

C.3. Measurements Through the Main Filter Slot Which is Not Occupied

In previous models of the ANA-971++ (ANA-951/ANA-961), the analog signal penetrated through other filters if the selected filter slot was empty (i.e., filter was not installed). This caused problems in measurements, because this kind of error was difficult to diagnose. This problem does not exist in the ANA-971++. Measurements through the empty slot will give the result as if there is no signal at the input.

APPENDIX D

BIT SHIFT (PHASE MARGIN)

NOTE: The bit shift analyzer is an optional board that must be installed by Guzik Technical Enterprises Manufacturing before delivery of your RWA-2550++.

D.1. Bit Shift

There are two classes of bit shift; **systematic** and **random**. Systematic bit shift is caused by interference of the read signal pulses. Random bit shift is caused by noise from many sources in the read and write channels.

D.2. Systematic Bit Shift

Refer to Figure 19. The two curves are voltage waveforms, with time along the X-axis and voltage along the Y-axis, both in the same scale.

When pulses are added, their slopes being overlapped with peaks of each other cause the peaks of the resulting waveform to be shifted versus their original location. At (**a**) is shown a positive and a negative read pulse close enough that the tails of their waveforms overlap with the peaks marked by arrows. At (**b**) is shown the sum of them. The peaks are shifted apart due to the addition of the slopes of both pulses. Pulse shape is affected by every element in the write/read process; although many of the elements in the read-write signal chain are individually non-linear, the entire process is very close to linear.

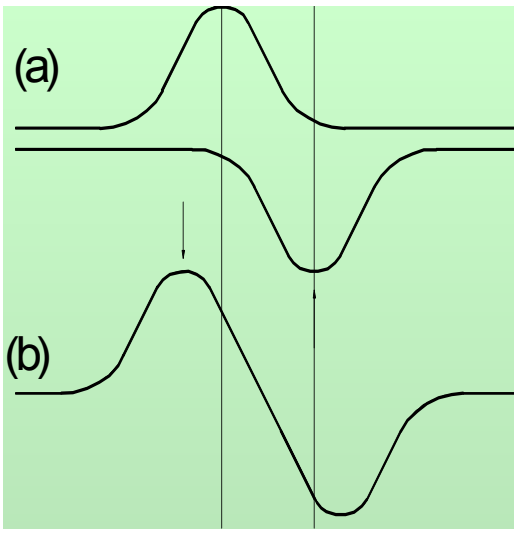


Figure 19 Systematic Bit Shift

D.3. Random Bit Shift

In the absence of the systematic bit shift, transitions are normally distributed around the centers of their bit cells, due to the noise in the read/write channel. Using σ as the distribution parameter, the expression

$$p(x) = \frac{2}{\sqrt{\pi}} \cdot e^{-x^2}$$

gives the density of probability that a data pulse comes at the distance $\sigma \cdot x$ from the center of its window. The cumulative probability of the peak position being farther than $\sigma \cdot x$ is Erfc(x) that in its turn can be closely approximated by

$$S(x) = \frac{2}{\sqrt{\pi}} \cdot e^{-x^2} \cdot \frac{1}{x}$$

A parabola can approximate the log (S(x)) for small error rates (4% accuracy for error rates below 0.034). The Bits Shift Analyzer directly measures the S(x), therefore the plot of error rate versus window size on the logarithmic scale should look like a parabola.

D.4. Combined Bit Shift

Figure 20 (a) shows a bit shift plot which combines the effects of both systematic and random bit shifts. For windows from 0 to 10 ns, the bit shift is clearly systematic, since error level is nearly constant and = 0 (i.e. all bits are in error). For windows > 10 ns, the effects of systematic and random bit shifts are combined, and the statistics of the random one effects on the shape of the curve. Figure 20 (b) shows a curve in which there is no systematic bit shift and random only is present.

D.5. Terminology

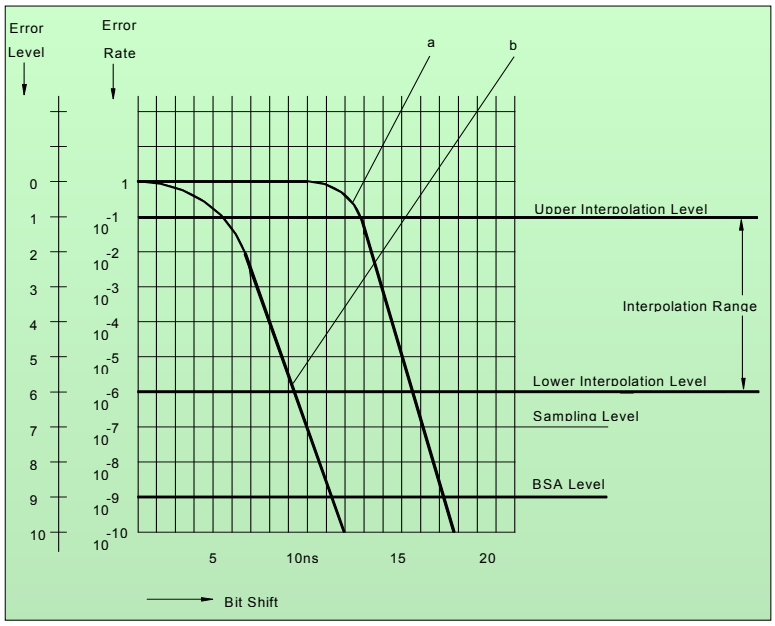


Figure 20 (a) is similar to the bit shift plot screen produced by software, but has additional features. Not everything shown in this figure appears on the plot. **Error level** is used to refer to logarithmic values, **error rate** is used for values not converted to the logarithmic scale.

The bit shift plot as presented by software has error level along its Y-axis, and window margin (in ns) along X-axis. There are several terms used in description of the bit shift measurement, which must be distinguished. Here are their definitions.

Figure 20 Combined Bit Shift

Error Level. Error Level = -log(Error Rate). When we need to specify a level (an ordinate or Y-value) on the BSA plot, we cannot refer to it as a BSA level, since this term is reserved for another specific meaning (see below).

Sampling Level. The sampling level is the logarithm of the maximum number of samples to be processed for each window setting. For example, if the sampling level is set to 7, then up to 10^7 samples may be obtained. Sampling is stopped when enough information has been gathered to calculate the BSA error rate.

BSA Level. The BSA level is the negative logarithm (base ten) of a selected bit shift error rate. Software computes the estimated bit shift for this error rate. Equivalently, we can say that if the window was set for

the estimated bit shift, we would expect to see a bit shift error rate with the negative logarithm equal to the BSA level. Software can use either linear or parabolic interpolation to build a bit shift curves. If linear interpolation is used, then the BSA level must be set between 0.0 and 9.0 inclusively. If a parabolic least square fit method is chosen, the BSA level may be set higher and extrapolation will take place.

Number of Window Settings. One quarter of the bit cell period is divided into this number of equal parts to perform any bit shift related test. Because window settings must be selected from a discrete set of values (provided by the BSA calibration table), the actual window settings will be different from calculated ones. Software is using these actual window settings to build bit shift plot and calculate the estimated bit shift.

Type of Fit. User can select either a simple linear interpolation method, or a parabolic least square fit. In linear interpolation method, data points are connected by segments of a straight line on the bit shift plot. In a parabolic least square fit, an approximating parabola is calculated using data points that fall within the user specified interpolation range (see further).

Linear Interpolation. In this method, adjacent data points are connected by segments of a straight line. If one of these segments crosses the BSA level, the intersection is calculated and the corresponding window is taken to be the estimated bit shift.

Parabolic Least Squares Fit. As the error rate decreases, direct calculation of the estimated bit shift becomes increasingly time consuming. By convention, the RWA-2550++ will only make direct measurements of error rates greater than 10^{-9}. The estimated bit shift, at error rates less than 10^{-9}, can be calculated by means of extrapolation using a parabolic least squares fit. The intersection of the BSA level with this parabola is the calculated estimated bit shift.

Interpolation Range. BSA plot is most near to a parabola when error rate is neither too high nor too low. Thus, we allow user to specify a range of BSA levels to be used for the parabolic fit. It is called the interpolation range. As with the BSA level the limits of the interpolation range are expressed as negative logarithms of the error rate. Only error rates in the interpolation range are used in calculation of the parabolic least squares fit.

Number of Window Settings for Interpolation Range. In the user specified interpolation range, one quarter of the bit cell period is divided into this number of equal parts to perform error rate measurements. The number of window settings inside and outside the interpolation range can be set separately. To improve parabolic curve fitting, the first one can be specified larger to get more measurements inside the interpolation range.

Acceptable Correlation Coefficient. This is used only with a parabolic least square fit only. User specifies a minimum acceptable correlation coefficient for the curve fitting. If the correlation coefficient of the curve fit is less than the specified value, the resulting estimated bit shift is not considered reasonable. But even in this case, a curve fit will be attempted and used for the calculation of the estimated bit shift.

APPENDIX E

THE READ CHANNEL FREQUENCY RESPONSE MEASUREMENT

The following is a procedure used for determining frequency response of four main filters in the ANA-971++ and the Read Channel.

NOTE: All references to menu items refer to WITE.

NOTE: All mentioned attenuator settings are specified for the read channel input signal of 50-mV p-p connected to the 50-Ohm output of the network analyzer. If you change the amplitude of the network analyzer output signal, adjust the attenuator to the appropriate setting, such that the read channel output signal from the ANA-971++ is less than 300 mV p-p single-ended on a 50 Ohm termination.

E.1. Using a Network Analyzer to Measure Main Filter Frequency Response

Perform the following actions to measure the main filter frequency response.

1. Perform a calibration of the BNC/BNC cable (see E.1.1).
2. Perform frequency response measurement of a non-programmable filter (see E.1.2).
3. Perform frequency response measurement of a programmable filter (see E.1.3).

E.1.1. Response Calibration for the Coax BNC/BNC Cable

The analog RDX/RDY IN data cable (Guzik Part Number 462490-A) is used by Guzik Manufacturing to calibrate the ANA-971++, and therefore is already calibrated. However, the cable used to connect the READ CH.OUT test point and the network analyzer is not pre-calibrated by Guzik Manufacturing, and must be calibrated before use.

Follow the instructions below to calibrate the response of the coax BNC/BNC cable:

1. Connect the READ CH.OUT test point with a coax BNC/BNC cable to the OUT connector on the front panel of the network analyzer. (See Figure 21.)
2. Connect the other end of the cable to the to the IN connector on the same network analyzer.
3. Perform network analyzer calibration through this cable.

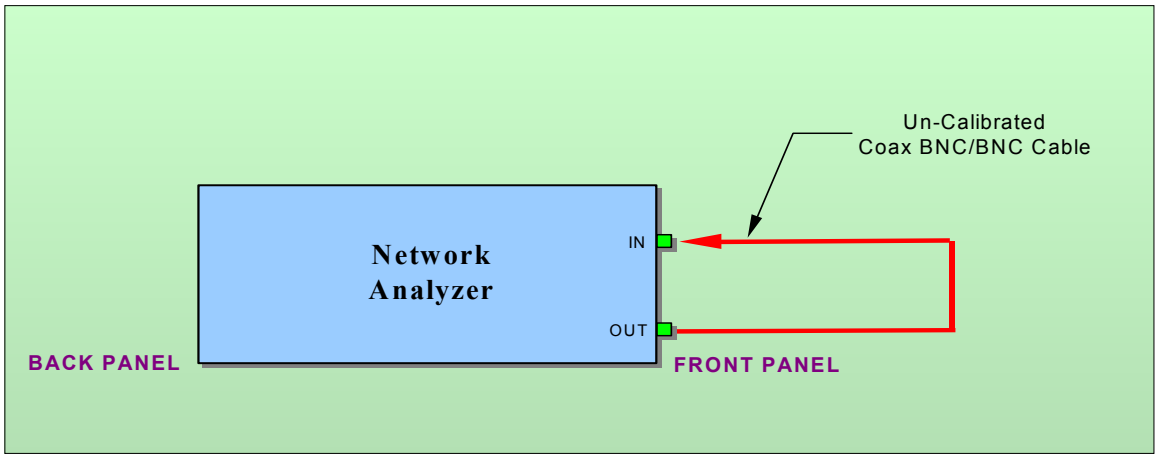


Figure 21 Coax BNC/BNC Cable Calibration Diagram

E.1.2. Main Filter Frequency Response Measurement

Follow the instructions below to measure the main filter frequency response:

1. Set the output level of the network analyzer to 50 mV p-p terminated to 50 Ohms.
2. Connect the output of the network analyzer to the ANA-971++ via the analog RDX/RDY IN data cable (Guzik Part Number 462490-A). To do this, disconnect it from the UP-7, terminate one of two differential inputs to 50 Ohms, and connect another one to the network analyzer (See Figure 22.).

   NOTE: Depending on the connector type of the network analyzer output, some adapter will be required to do this. It makes no difference which input (X or Y) you will be using, unless there are no hardware problems in the read channel.

3. Connect the READ CH. OUT test point on the front panel of the ANA-971++ to the **50-Ohm** terminated input of the network analyzer with the coax BNC/BNC cable that has been calibrated.

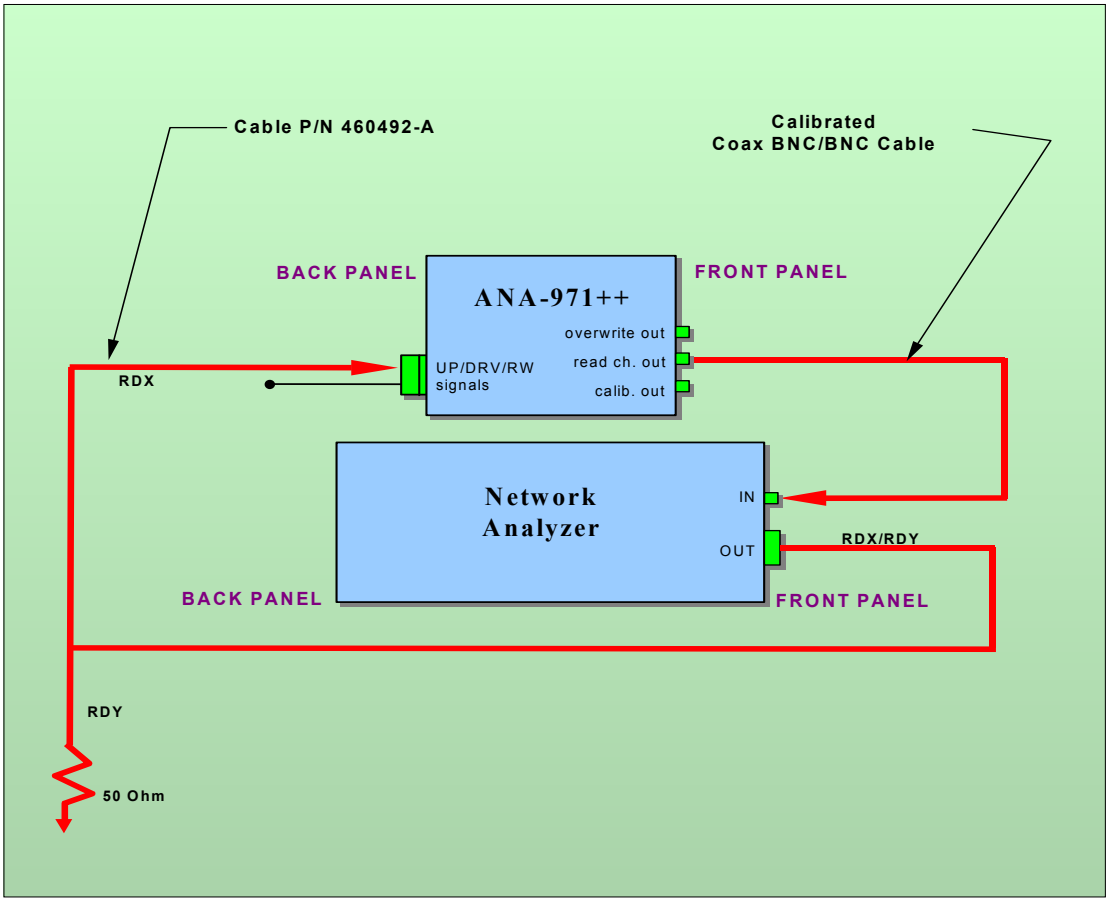


Figure 22 ANA-971++ & Network Analyzer Connection Diagram

4. Place the filter to be tested into any filter slot on the main filter matrix board.
5. Start WITE.
6. Select the proper filter position using Control | Filter Menu in WITE engineering mode.
7. Set the main attenuator to position 2 using Control | Gain Menu.

8. Measure the frequency response of the filter using the network analyzer.

To measure the frequency response of the analog channel, use an open filter and follow the procedure described above.

E.1.3. Programmable Filters

1. Set the output level of the network analyzer to 50 mV p-p terminated to 50 Ohms.
2. Connect the output of the network analyzer to the ANA-971++ via the analog RDX/RDY IN data cable. To do this, disconnect it from the UP-7, terminate one of two differential inputs to 50 Ohms and connect another one to the network analyzer. (See Figure 22.)

   NOTE: Depending on the connector type of the network analyzer output, some adapter will be required to do this.

3. Connect the READ CH. OUT test point on the front panel of the ANA-971++ to the **50-Ohm** terminated input of the network analyzer with the coax BNC/BNC cable that has been calibrated.
4. Place the filter to be tested into the main filter matrix board slot.
5. Start WITE.
6. Select the proper filter position using Control | Filter Menu.
7. Select the proper parameters for the programmable filter using the Control | Filter Menu.

   NOTE: The cut-off frequency will depend upon the filter type installed.

8. Set the main attenuator to position 2 using Control | Gain Menu.
9. Measure the frequency response of the filter using the network analyzer.
10. Set the programmable filter BOOST to 6 dB using Control | Filter Menu.
11. Measure the frequency response of the filter using the network analyzer.

    NOTE: The frequency response of a programmable filter can be measured for any combination of cut-off frequency and boost factor. However, if the BOOST is set to more than 6 dB, the position of the main attenuator should be changed to 6.

APPENDIX F

THE PATTERN GENERATOR

F.1. Pattern Generator

A **pattern generator** is a special processor that outputs the stream of zeroes and ones, accompanied with bit mask and precompensation interpretation. Any "1" bit can be precompensated, and any bit cell can be masked.

Precompensation (or precomp) means shifting data pulse in time versus its normal position, i.e. output it earlier or later than usual. Precompensation is used in magnetic recording to eliminate transition shifts due to pulses' interference.

A user can define patterns of test data. **Patterns** are defined in terms of encoding scheme and sequences of zeroes and ones that can be repeated several or infinite number of times. The data stream generated is used as write data during write operations, or as a reference during read operations.

Pattern definition is stored in the pattern generator's memory. The pattern memory can store up to 32K bytes of encoded data.

A user constructs a custom data pattern by repeating one (or more) pre-defined patterns a specified number of times, or by concatenating individually-defined patterns, or a combination of both. Custom data pattern creation is performed using the pattern editor, in the WITE software.

For more detailed information about Pattern Definition Language see the *WITE User's Guide*.

APPENDIX G

COMPARATIVE DESCRIPTION OF THE TWO PATTERN FILE COLLECTIONS

G.1. Definitions

There is a new pattern file collection included in 32-bit releases of WITE. The recently introduced RWA-2550++ and earlier RWA models (1601, 1632, 1001 and their modifications) therefore have different pattern files collections. The old pattern files intended for earlier models are referred to here as the **1601 collection,** while the new pattern files are referred to here as the **2550++ collection.**

G.2. Pre-Requisite

Pattern files are a complicated, detailed subject. Before attempting to understand this appendix, please read the appropriate sections of the *WITE User's Guide*.

G.3. Purpose of the Appendix

The audience for this appendix is programmers/test engineers who want to customize 2550++ pattern files, or programmers/test engineers who want to re-code 1601 pattern files in a coding style similar to the 2550++ pattern files.

If you are unfamiliar with patterns, use section G.5 as a reference for definitions of 2550++ patterns. Also, use G.5 as a listing of the 2550++ patterns that are available.

If you have previously customized 1601 pattern files, and you now intend to create a new customized 2550++ pattern file, you want to know about the differences between the 1601 pattern file collection and the 2550++ collection. You will find in this appendix a comparison between how the 1601 pattern files were coded (and why) and how the 2550++ pattern files were coded (and why). You can use this understanding to customize a 2550++ file in the new coding style.

If you plan to re-code a 1601 pattern file in the new 2550++ coding style, you need to read this appendix. 1601 pattern files that have been customized operate well on the 2550++. There is little reason to consider re-coding these customized 1601 pattern files, unless you want to take advantage of the new 2550++ coding style benefits and new WITE capabilities. This appendix discusses the major differences between the two pattern collections in an effort to assist you in making the decision whether to re-code, and figuring out the way of performing the conversion from 1601 pattern file coding to 2550++ coding.

G.3.1. Introduction

The 2550++ pattern file collection, featuring major EP2 and PD2 extensions, is introduced in WITE. The 2550++ pattern file collection is intended to be used only with the 2550++ machine. The 1601 EPT / PDL pattern file collection is intended to be used with earlier RWA models (the 1601 pattern file collection is included in WITE for that purpose).

It is useful to understand the three major reasons why the new 2550++ pattern file collection has been created:

1. The new 2550++ pattern generator has no restriction for programming consecutive transitions. This makes it unnecessary to support the two 1601 collection pattern sets ("single" and "double"). Single and double pattern terminology is now obsolete.
2. WITE allows more than one pattern file to be loaded at a time. This makes it unnecessary to support the "all in one" pattern file design approach used in the 1601 collection, eliminating one major reason for customizing the pattern files.
3. An analysis of the 1601 collection showed that the minor extension of Pattern Description Language (PDL) would allow re-design of the pattern files, avoid excessive copying, and, thus, producing more compact, observable and maintainable pattern files.

Guzik Technical Enterprises decided to create a new 2550++ pattern collection and leave the 1601 pattern collection (targeted for earlier models) unchanged. As a result, the 2550++ collection:

- does not support single or double pattern flavors, and thereby reduces the number of patterns by half from the equivalent 1601 pattern file collection
- is designed to comply with the WITE multiple pattern file selection facility, reducing substantially the need to customize the 2550++ pattern files, and further, reducing redundant code (necessary in the 1601 pattern file collection where only one pattern file could be selected)
- uses a pattern template definition approach, generating standard sets of patterns intended for different hardware channels from the same set of pattern templates (and as a result, the new pattern files code looks substantially different from the 1601 pattern files)

The differences between the 1601 pattern collection and the 2550++ collection are stylistic: both collections are compilable by the same PDL compiler (starting from version 1.4) and result in the same EPT specification binaries. Pattern files from the 1601 collection can be loaded and used for the RWA-2550++.

G.4. 1601 Patterns Collection

Standard configurations of earlier RWA models featured a pattern generator that was unable to play bit sequences with no zeros between transitions.

For example, the sequence "01010010" was allowed, while "01101010" was prohibited. As a result, patterns written for the standard configuration feature maximum flux reversal frequency twice lower than a bitcell frequency. These patterns are referred to as "single patterns".

Optionally, earlier RWA models have been being equipped with an advanced "double" pattern generator (double-PG). Double-PG does not have the "two consequent transition" restriction. Accordingly, patterns designed for the "double" pattern generator feature flux reversal frequencies up to bitcell clock. Patterns for the double PD are referred to as "double patterns".

The 1601 collection includes both single and double pattern sets to get the maximum performance from both configurations. With a few exceptions, both single and double flavor for any particular pattern is available. The name of "double" pattern differs from the single counterpart by letter "D", used as prefix, postfix or in the middle of the pattern name.

Here are few examples of single and double patterns, available in the 1601 collection:

Pattern	*Single Flavor*	*Double Flavor*	*Pattern file*
High Frequency	HF, "01010101"	HFD, "11111111"	patterns.pdl –HF, hfprm.pdl – HFD, nlts.pdl –DHF
		DHF, "11111111"	
Worst Case	WC	no double flavor	patterns.pdl
Low Frequency	LF,"10001000"	LFD," 10101010"	patterns.pdl – LF, hfprm.pdl -LFD
Fifth Harmonic, NLTS	HRM5	DHRM5	NLTS.PDL

Table 24 1601 Pattern Files - Single and Double Pattern Examples

As a rule, the single and double flavors feature the same signal shape, with the data rate two times higher for a double flavor. This data rate difference is programmed either explicitly in the pattern bit sequence (the way it is used for peak detection and native Guzik PRML channel patterns, HF example in the above table) or, controlling channel clock frequency through dblwclk scheme pragma (the way, used for integrated PRML chip patterns, DIGital mode).

Accordingly, two sets of schemes, single and double, are supported. Single patterns are based on single schemes while double patterns on double schemes.

The following table shows the examples of scheme flavors:

Scheme Description	*Single Flavor*	*Double Flavor*
Peak Detection, no encoding	NRZ	RWAD
Guzik PRML, PR4	GPR4	GPR4D
Read/Write through Guzik, Clock from SSI4910 integrated PRML chip	SSI4910NRZ	SSI4910M
Read, Write and Clock through SSI4910 integrated PRML chip (Digital channel)	SSI4910C	SSI4910D

Table 25 1601 Pattern Files - Scheme Flavor Examples

G.5. 2550++ Patterns Collection

The "consequent transitions" restriction has been relaxed with introduction of RWA-2550++ with its new pattern generator. As a result, 2550++ collection no longer needs to support both pattern sets: single patterns became obsolete.

The 2550++ pattern collection does not attribute its patterns as "single" or "double". It has been constructed from the 1601 collection in the following way:

G.5.1. Parametric Patterns

The following six standard parametric patterns are available:

Pattern Name	Pattern Contents
FF	"1111111111111111"
HF	"1010101010101010"
LF	"1000100010001000"
RF	"1000000010000000"
IS	"1000000000000000"
WC	0xB6D9 /MFM encoding

Table 26 Six Standard Parametric Patterns

Defined in: *param.pdt*

Available in: *param.pd2*

The first five of the patterns are referred to as frequency patterns.

1601 and 2550++ patterns with the same names deliver the same bit sequences on the same data rate. The following table represents 1601 and 2550++ patterns producing equivalent signals (with generally speaking, different preambles):

2550 Collection	1601 Collection
FF	HFD,DHF
HF	HF,LFD
LF	LF
RF	ISD
IS	IS
WC	WC

Table 27 Scheme Flavor Examples

In contrast with 1601 patterns, 2550++ frequency patterns are based on the RWAD scheme to emphasize the absence of the “consequent transitions” restriction.

G.5.2. Standard Chip Patterns

The following are the standard chip patterns.

G.5.2.1. Read/Write Through Guzik, Clock from Chip

The following two standard patterns available:

Pattern Name	*Pattern Type*
PPRMD	low frequency
PRNDD	Pseudorandom

Table 28 Read/Write Patterns

Defined in: *cad.pdt*

Available in: *all chip specific pattern files*

G.5.2.2. Digital Channel

The following four standard patterns are available:

Pattern Name	*Pattern Type*
P0D	"0"*INF
P1D	"1"*INF
PCTRD	Counter
PCTR10D	"bad" Counter (10 bit per write gate difference with Counter pattern)

Table 29 Digital Channel Patterns

Defined in: *cad.pdt*

Available in: *all chip specific pattern files*

G.5.3. NLTS Pattern

The 2550++ NLTS pattern set is a 1601 NLTS double set. The letter "D" can either prefix or postfix the pattern name, exactly as in the 1601 collection. This style has not been changed to support test code compatibility and compatibility with customer's patterns, modified for Guzik standard tests.

In contrast with other groups, NLTS patterns are not specified in test setups in most cases. Instead, they are selected indirectly by specification of measurement type or method. Patterns are categorized by the test in which they are used. Few patterns are used in more than one test.

Pattern for Pulse Match has been dropped along with a test.

G.5.3.1. Spectral Elimination

```
HRM5D, HRM5R
HRM5AD, HRM5AR
HRM3D, HRM5R
```

G.5.3.2. Alternative Spectral Elimination / NLTS vs. Write Current

```
DHRM5, DHRM5N, DHRM5V, DHRM52, DHRM52N, DHRM53, DHRM53N, DHRM5R, DHRM5RR
```

G.5.3.3. Pseudorandom

```
RND730D
```

G.5.3.4. MR Transfer Curve

```
DLLF, DL5F
```

G.5.3.5. Third Harmonic Ratio

```
DLLF, DHF
```

Defined in: *NLTS.pdt*

Available in: *NLTS.pd2*

G.6. Pattern Files Organization

The following describes the overall organization of the pattern files, and describes the differences between the 1601 pattern collection and the 2550++ collection.

G.6.1. 1601 Pattern Collection

As a rule, patterns are defined immediately inside pattern files. A pattern description contains a set of attribute assignments, defined explicitly or inside a INC file, included in the appropriate place of a pattern description. All referenced schemes are defined inside the `schemes.sc` file, which should be included in pattern file before the first pattern description.

G.6.1.1. An Example of a 1601 Pattern Definition

Below is an example of a 1601 pattern definition:

```
patdef IS
        scheme = NRZ
        pattern = 0X8000*INF
patend

patdef PPRM
        #include "vnm416n.inc"
        pattern = "1000100010001000"*INF
patend
```

G.7. 1601 File Types

The 1601 collection comprises files of four types:

- EPT files – pattern files in WITE-readable form, the result of PDL files compilation.
- SC files – scheme files. The only scheme file **schemes.sc** can be found in a WITE root directory.

- INC files - include files. These files do not have any special semantic beyond bringing their content into specific places of PDL program via #include directive. INC files are stored in the WITE root directory. De facto, they are used to hold definitions of extensive bit sequences, or collections of pattern attributes used from pattern to pattern.

- PDL files – pattern files, compilable to WITE readable form (EPT files). They are stored in the product directory. The following standard files are available:

Pattern Name	*Pattern Type*
patterns.pdl	parametric measurements with single PG
hfprm.pdl	parametric measurements with double PGs
NLTS.pdl	nonlinear transition shift measurements
PRML4910.pdl	PRML tests, Guzik internal and integrated SSI4910 PRML chip.
Vnm416.pdl	PRML tests, Guzik internal and integrated VENOM PRML chip.

Table 30 The 1601 Collection Standard Pattern Files

NOTE: Pattern files for other integrated PRML chips are also available.

G.7.1. 2550++ Collection

In contrast with the 1601 collection, most standard 2550++ patterns are defined in the following form:

```
patdef  PatternName
         cntrl    = CntrlBlkName
         pattern  = Bit Sequence
patend
```

That style of pattern definition is called the **pattern template**. Pattern template definition features the two attributes: pattern (which is a bit sequence to be played) and control-block (a named collection of any other attributes to be specified for a pattern). Usually, a control block comprises the pattern's hardware channel dependent attributes.

In order to make a pattern template compilable, a control block with a specified name must be specified prior to the pattern template definition.

Pattern templates are collected in pattern definition template (PDT) files, defined by the testing goals they are designed for (parametric measurements, NLTS measurements, integrated PRML chip testing).

Control blocks are collected in CB files. CB files are defined by the intended hardware channel (peak detection, specific integrated PRML chip, etc.).

2550++ pattern files (PD2 files) define patterns instantiating pattern templates from a specified PDT file by control blocks from a specified CB file.

G.7.1.1. Example of PD2 file:

```
;Param.pd2 - parametric patterns for RWA-2550++ machine

#include "bits.gdf"   ; standard bit sequences
#include "schemes.sc" ; pattern schemes

#include "param.cb"   ;peak detection  control blocks
#include "param.pdt"  ;parametric pattern templates
; end of param.pd2
```

G.7.1.2. Example of Control block file:

```
;Param.cb - control blocks for peak detection mode
ctldef ctlSTD
         scheme =RWAD
         preamble =  "00000000"*3.6us +
                                  "0101010101010101"*36.4us +
                     "0101010101010100"
         am_length = 2
ctlend
; end of param.cb
```

G.7.1.3. Example of Pattern Definition Template File

```
;PARAM.pdt    - parametric pattern templates for RWA-2550++ machine
;(excerption)
;This file is NOT compilable!

patdef HF
cntrl    = ctlSTD
pattern = bHF              ;"10101010"*INF
patend

patdef IS
cntrl    = ctlSTD
pattern = bIS              ;"1000000000000000"*INF
patend
; end of excerption from param.pdt
```

Beyond the instantiation of pattern templates, pattern files may have any number of pattern definitions in any PDL-allowable form.

G.8. The 2550++ Collection File Types

The 2550++ collection features seven different file types: SC, GDF, CB, PDT, INC, PD2 and EP2.

- EP2 files (Extended Patterns for RWA-2550++) - A compilation result of corresponding PD2 file, ready to be loaded to WITE

Location: product directory

- PD2 files (Pattern Definitions for RWA-2550++) - A collection of pattern definitions, ready to be compiled by PDL compiler, and the following are now available:

Pattern Name	*Pattern Type*
Param.pd2	parametric patterns for peak detection channel
NLTS.pd2	non linear transition shift measurement patterns
SSI4910.pd2	patterns for ssi4910 and compatible integrated PRML chips
VNM416.pd2	patterns for Venom and compatible integrated PRML chips

Location: product directory

Table 31 The 2550++ Collection Standard Pattern Files

NOTE: Pattern files for other integrated PRML chips are also available.

- PDT files (Pattern Definition Templates) - A collection of pattern templates, and currently three pattern template files are available:

Pattern Name	*Pattern Type*
Param.pdt	standard parametric pattern templates
NLTS.pdt	standard NLTS pattern templates
CAD.PDT	standard pattern templates for integrated PRML chip)

Location: WITE root directory

Table 32 PDT Patterns

- CB files (Control Blocks) - A pattern control blocks.2550++ pattern collection comprises a standard CB file, along with one CB file per integrated PRML chip (VNM416.CB, SSI4910.CB and so on)

Pattern Name	*Pattern Type*
Param.cb	control blocks for Peak Detector channel

Location: WITE root directory.

Table 33 CB Patterns

- GDF files (Guzik Data File) - The extension is used for miscellaneous data files. 2550++ collection has the only GDF file, **BITS.GDF**, which contains almost all named bit sequences in use (except preambles and some specific sequences)

Location: WITE root directory.

- SC files (SChemes) - The pattern schemes. 2550++ pattern collection utilizes the only scheme file **SCHEMES.SC**, which is exactly the same as in 1601 collection

Location: WITE root directory.

- INC files (INClusions) - The supplementary files, containing raw lines of PDL statements to be included in appropriate places of PDL program using #include directive; recently, the 2550++ collection utilizes only two INC files: **random.inc** and **randomd.inc** containing extensive random bit sequences for PRML random patterns

Location: WITE root directory.

G.9. Pattern Files and Multiple File Loading

G.9.1. 1601 Pattern Collection

The 1601 collection was designed with the assumption that only one pattern file is loaded into WITE at a time. Every file is supposed to contain a broad set of patterns, required for this or that testing objective. Due to a diversity of objectives, standard pattern files are intended only for the most common ones:

Pattern Name	*Pattern Type*
patterns.pdl	parametric measurements with single PG
hfprm.pdl	parametric measurements with both single and double PGs
NLTS.pdl	nonlinear transition shift measurements
PRML4910.pdl	PRML testing using Guzik internal and integrated SSI4910 PRML chip.
Vnm416.pdl	PRML testing using Guzik internal and integrated VENOM PRML chip.

Table 34 1601 Pattern Collection

NOTE: Pattern files for other integrated PRML chips are also available.

With the 1601 patterns, you were urged to create your own pattern files, putting together all patterns needed to accomplish your specific goals.

Loading a pattern file from the 1601 collection in combination with any other pattern file from the 1601 or 2550++ collection will most likely (but not necessary) lead to pattern names conflicts.

G.10. 2550++ Pattern Collection

The 2550++ collection is designed after the multiple pattern file loading features became available in WITE. Accordingly, a 2550++ pattern file contains a smaller set of the goal-oriented patterns than a standard or customized 1601 pattern file.

Selected combinations of pattern files may be loaded. Customers can create their own pattern files, adding them to a selected combination of standard files or replacing any of standard files.

The following standard pattern files are available:

Pattern Name	*Pattern Type*
Param.pd2	patterns for parametric measurements
NLTS.pd2	Nonlinear transition shift measurements
SSI4910.pd2	PRML measurements using integrated SSI4910 PRML chip
VNM416.pd2	PRML measurements using integrated VENOM PRML chip

Table 35 2550++ Standard Pattern Collection

NOTE: Pattern files for other integrated PRML chips are also available.

Any combination of standard pattern files (featuring not more than one integrated PRML chip pattern file) can be loaded into the system, guaranteeing that there are no name conflicts.

G.10.1. Name Conflicts

A name conflict can happen if more the one pattern with the same name is encountered during the loading of pattern files. If the loader encounters a pattern with a name already registered as loaded, the newer pattern with the same name will not load. When this situation occurs, an error message is displayed. After the user acknowledgement, the loader continues with the next pattern.

Name conflicts may appear if:

- A pattern file from the 1601 collection is loaded in a combination with any other pattern files: 1601 pattern files were designed with the assumption that only one pattern file can be loaded in at a time
- more than one integrated PRML chip pattern file from the 2550++ collection is checked to be loaded: PRML chip pattern files contain similar pattern sets, dedicated to *alternative* integrated PRML chip channels
- a user created pattern file contains one or more patterns with the same name as in other loaded pattern files

Guzik does not recommend loading a combination of pattern files with duplicated pattern names. If you find that you have duplicate names, either exclude the files causing the conflict or customize them (removing or renaming duplicated patterns).

APPENDIX H

CONTROL BLOCKS CATALOG

The following standard control blocks are available:

Control Block Name	*Description*	*Where Defined*	*Scheme Featured*
ctlSTD	Standard Control block for peak detection mode	param.cb	RWAD
ctlPCMP	Read/Write through Guzik, clock from integrated PRML chip	PRML Chip dedicated CB file, e.g.: SSI4910.cb – for SSI4910, VNM416.CB – for VENOM	"M" postfixed chip specific scheme, e.g. SSI4910M, lpr416m
ctlDIG	Read, Write and Clock through integrated PRML chip (Digital mode)	PRML Chip dedicated CB file, e.g.: SSI4910.cb – for SSI4910, VNM416.CB – for VENOM	"D" postfixed chip specific scheme, e.g. SSI4910D, lpr416d

Table 36 Control Blocks Catalog

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