ADP7104 Digitizer

Datasheet

Key Features

- 10-bit ADC resolution
- 2 channels at 32 GSa/s with DC to 10 GHz analog bandwidth
- 4 channels at 16 GSa/s with DC to 6.5 GHz analog bandwidth
- Input sensitivity of 16 mV to 8 V peak-to-peak full scale
  - Selectable with 1 dB calibrated sensitivities
- SFDR -70 dBc @ 1 GHz
- ENOB 6.5 @ 1 GHz, full analog bandwidth 6.5 GHz, -3 dB full scale
- Channel digital triggers
- External digital trigger
  - Jitter < 1 ps RMS
- 128 GByte on-board memory (upgradeable to 256 GByte)
- Real-time digital full-band frequency and phase response equalization
- Digital real-time low-pass filter (LPF)[1] with adjustable bandwidth
  - Decimation by 2, 4, 8, 16, 32 or 64
- Real-time Digital Down Converter[1] with maximum span of 2.5 GHz and down to 38.1 kHz
  - Decimation by 10 to 10×2^{16} (32 GSa/s mode) or 5 to 5×2^{16} (16 GSa/s mode)
- Real-time Averaging[1] with external trigger
- Segmented memory acquisition[1] with minimum dead-time of 200 nanoseconds
- Channel-to-channel skew less than ±2 ps
- Multiple ADP7104 digitizers synchronization[1]
- Signal (time-domain) and spectrum analyzer (frequency-domain) display with software control panel
- Data transfer to computer with speeds up to 10 GB/s

Overview

The Guzik ADP7104 is a 10-bit, 32 GSa/s digitizer that combines adjustable frontends, high-speed ADCs and built-in FPGA digital signal processing, which enables signal capture and analysis with high-throughput data transfer to host computer of up to 10 GB/s. The ADP7104 comes in a display-less 19” Guzik enclosure.

[1] Optional software license

Front Panel

The front panel of ADP7104 is shown in Figure 1 and Figure 2. The following connectors are accessible on the front panel.

Figure 1. ADP7104 Guzik Enclosure Front Panel

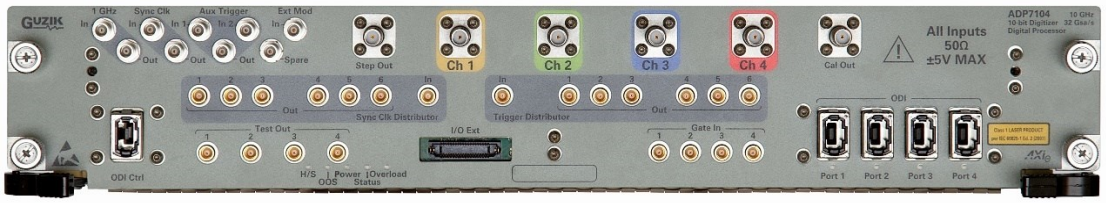

Figure 2. ADP7104 Module Front Panel

Ch 1, Ch 2, Ch 3, Ch 4	Analog inputs of the digitizer, SMA connectors
1 GHz In	Reference clock input.
1 GHz Out	Reference clock output.
Sync Clk In	Reference signal input to synchronize internal OCXO-based clock generator. The frequency of this signal is programmable from 10 MHz to 400 MHz and low jitter is required.
Sync Clk Out	100 MHz clock for external devices synchronization. It can be used to synchronize other digitizers.
Aux Trigger In 1, 2	External trigger input. This trigger should have low jitter and a slew rate ≥ 4 V/ns. The maximum frequency (for 100% trigger utilization) is 3.5 MHz. The trigger signal is converted to the digital domain and has jitter < 1 ps RMS.
Aux Trigger Out	Output signal to trigger external devices.
Spare	Reserved connector.
Sync Clk Distributor In	Clock signal input for clock distributor. Low jitter and slew rate less > 4 V/ns are required.
Sync Clk Distributor Out 1, 2, 3, 4, 5, 6	Clock signal output from clock distributor. These signals have low skew, low jitter and slew rate > 4 V/ns. They are used for multi-digitizer synchronization.
Trigger Distributor In	Trigger signal input to trigger distributor. Low jitter and slew rate > 4 V/ns are required.

Trigger Distributor Out 1, 2, 3, 4, 5, 6	Trigger outputs from trigger distributor. These signals have low skew, low jitter and slew rate > 4 V/ns. They are used for multi-digitizer synchronization.
ODI Port 1, 2, 3, 4	Optical interface for data streaming (up to 20 GB/s per port)
ODI Ctrl	Optical interface for data streaming and digitizer control (up to 10 GB/s).
Gate In 1, 2, 3, 4	Control signal which can start acquisition. The maximum frequency is 100 MHz and is reclocked on a sub-harmonic of sampling frequency 16 GHz / 80 = 200 MHz.
Test Out 1, 2, 3, 4	Output signal from FPGA for optional synchronization.
I/O Ext	Reserved connector.
LED Indicator	Power LED – solid green: normal. Can show under voltage or over voltage of digitizer power supplies. Overload LED – ADC overload, solid green is normal, solid red is overload. In case of overload the amplification is reduced to prevent ADC damage. The required amplification can be adjusted manually or automatically from Signal Display Control panel. Status LED – Solid green is normal. Red or orange indicates critical temperature or over temperature of digitizer components. For more information, see ADP7000 Digitizer User's Guide.

Block Diagram

The ADP7104 block diagram is shown in Figure 3.

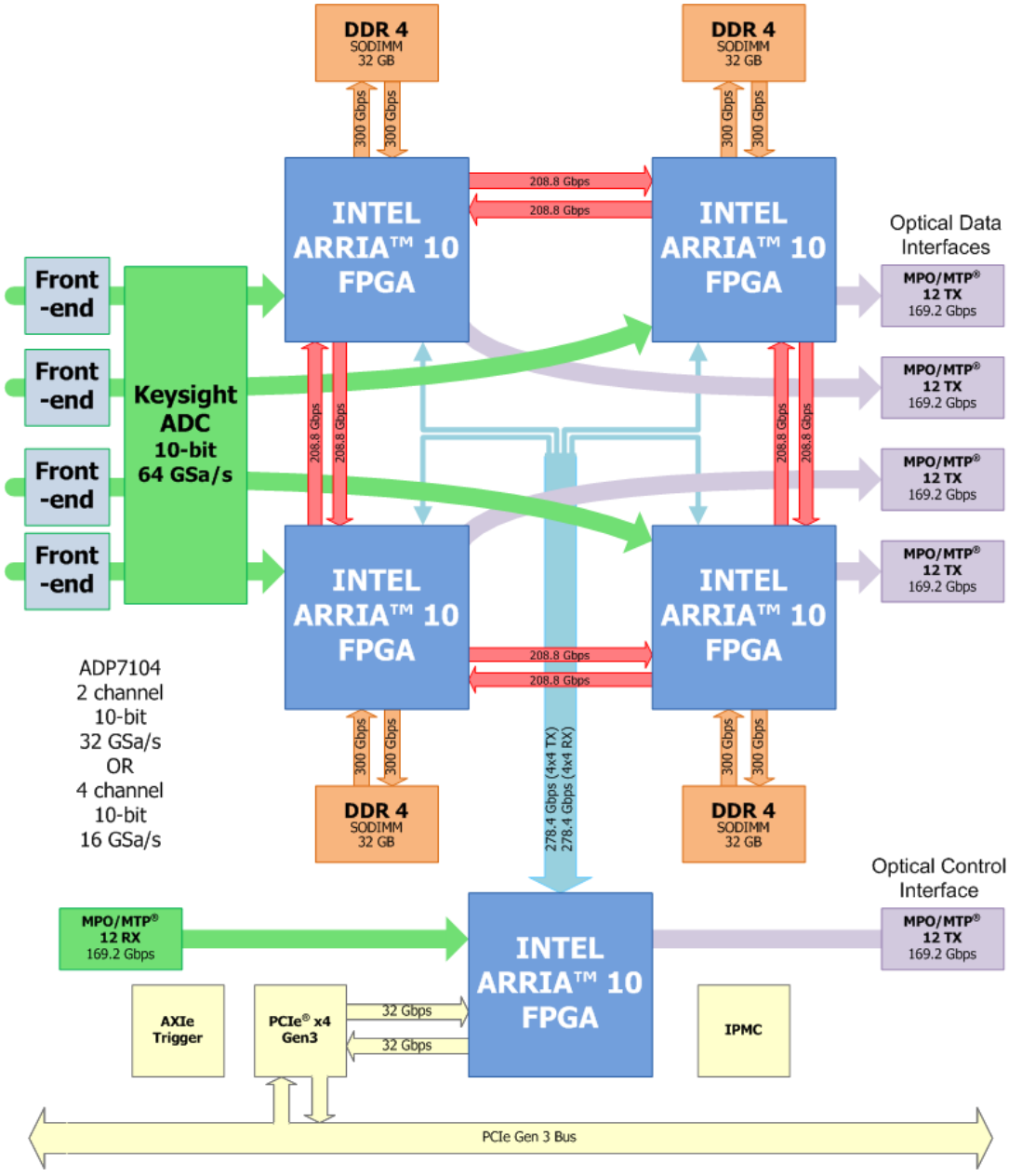

Figure 3. ADP7104 block diagram

Adjustable Frontend

The adjustable frontend enables the digitizer to work with input signals in the range 16 mV_{pp} to 8 V_{pp} (-32 dBm to +22 dBm) without external amplifiers or power dividers. Moreover, the wide range of DC offset adjustment allows the digitizer to work with maximum sensitivity in presence of DC voltage up to ±5 VDC. The gain of the frontend is calibrated with 1 dB steps.

Synchronous Acquisition

The four channels are synchronized during signal acquisition: they use a common 16 GHz clock and share the same trigger. The skew between channels is calibrated to the value < ±2 ps for all channel sensitivities. Therefore, the channels can be used with different sensitivities while maintaining a skew < ±2 ps. Figure 4 and Figure 5 shows the skew between channels vs sensitivity for 32 GSa/s mode and 16 GSa/s mode, respectively.

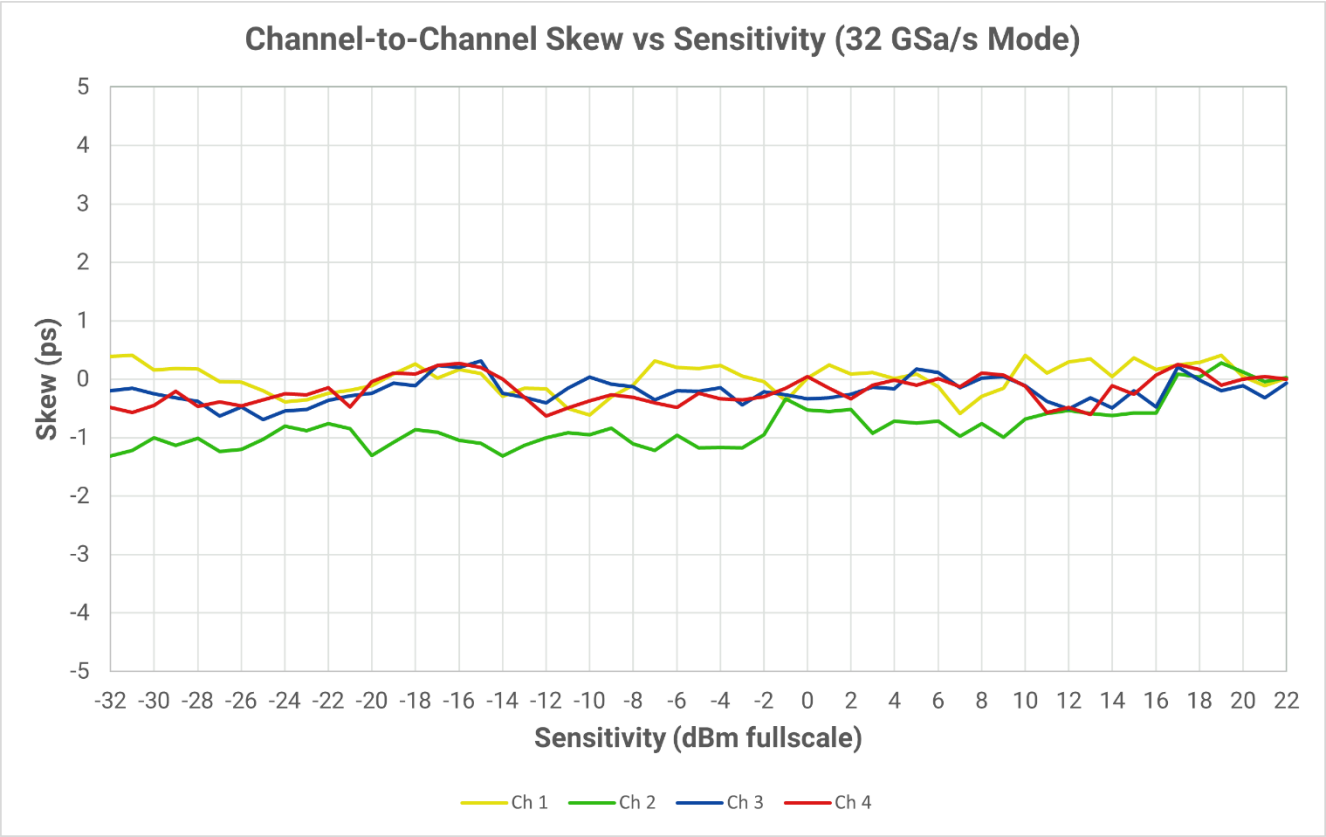

Figure 4. Channel-to-channel skew versus sensitivity with 32 GSa/s mode

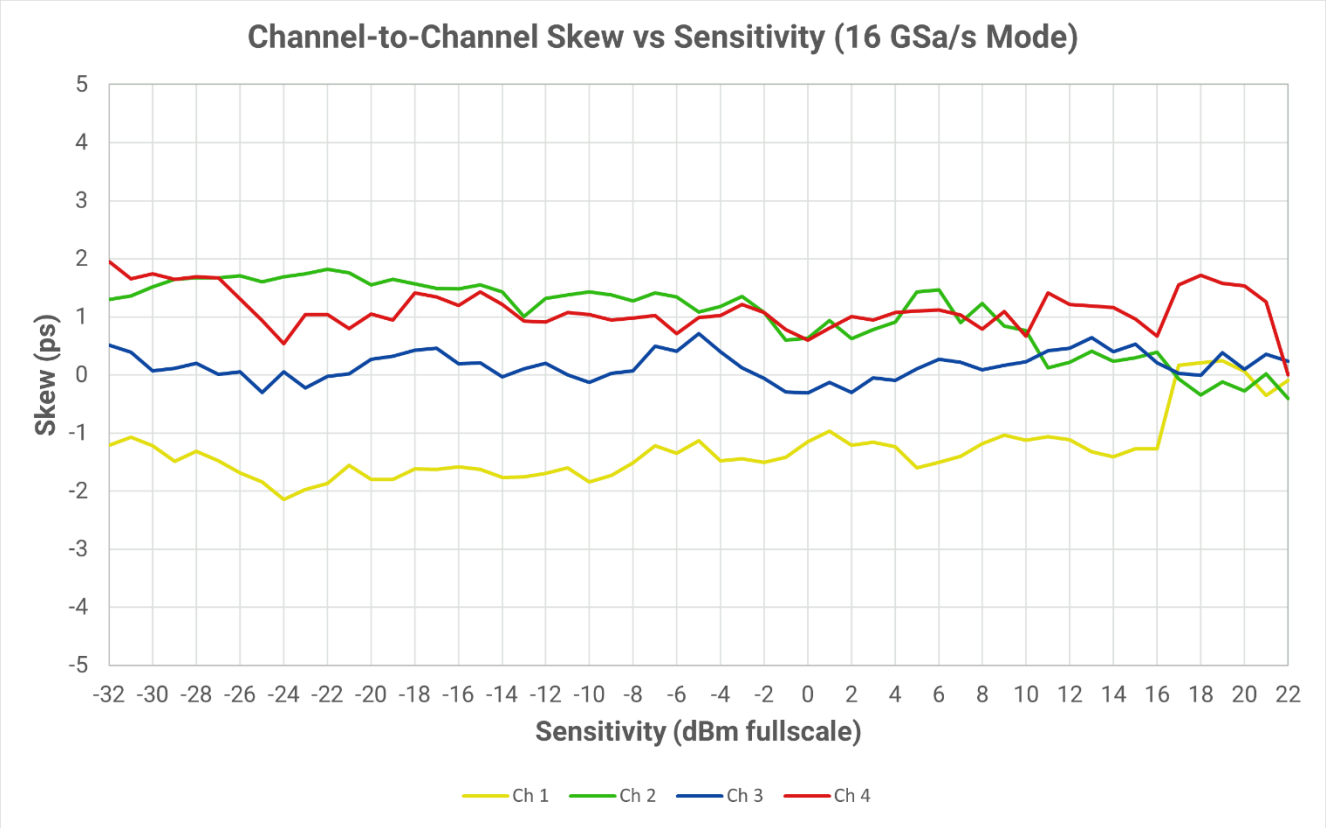

Figure 5. Channel-to-channel skew versus sensitivity with 16 GSa/s mode

Multi-Digitizer Synchronous Acquisition

Multiple digitizers can be used together to increase the number of channels for synchronous acquisition. The digitizers share a common reference clock and share the same trigger as shown in Figure 6. The skew between channels is calibrated to the value < ±5 ps for all channel sensitivities. Therefore, the channels can be used with different sensitivities while maintaining a skew < ±5 ps. Figure 7 and Figure 8 shows the skew between multiple digitizers' channels vs sensitivity for 32 GSa/s mode and 16 GSa/s mode, respectively.

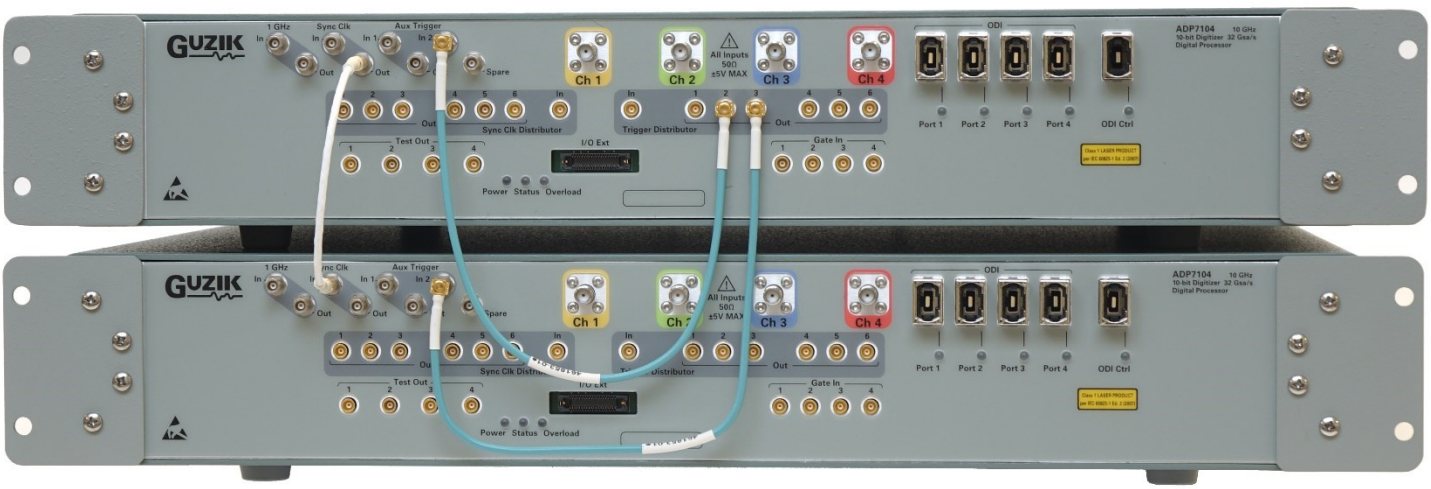

Figure 6. Multi-digitizer setup

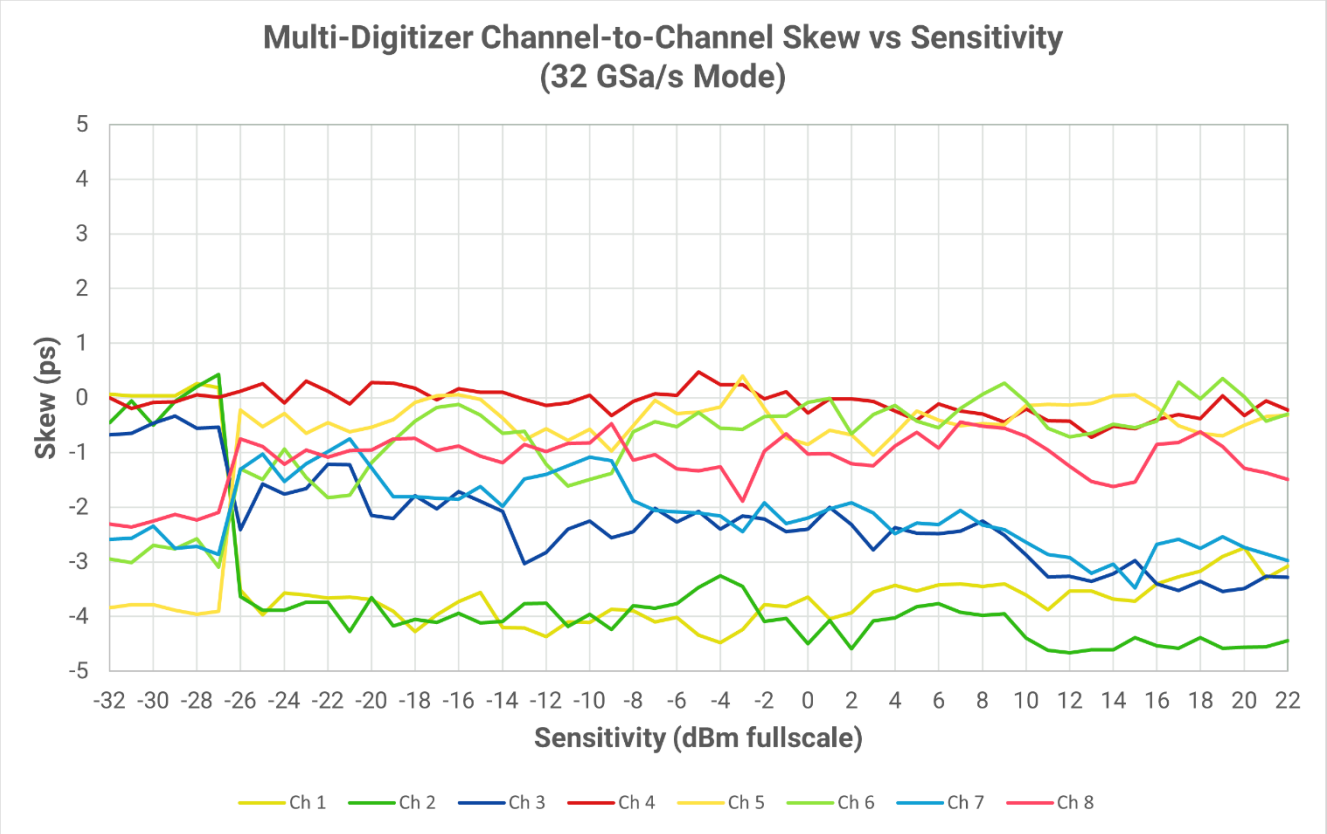

Figure 7. Multi-digitizer channel-to-channel skew vs sensitivity (32 GSa/s mode)

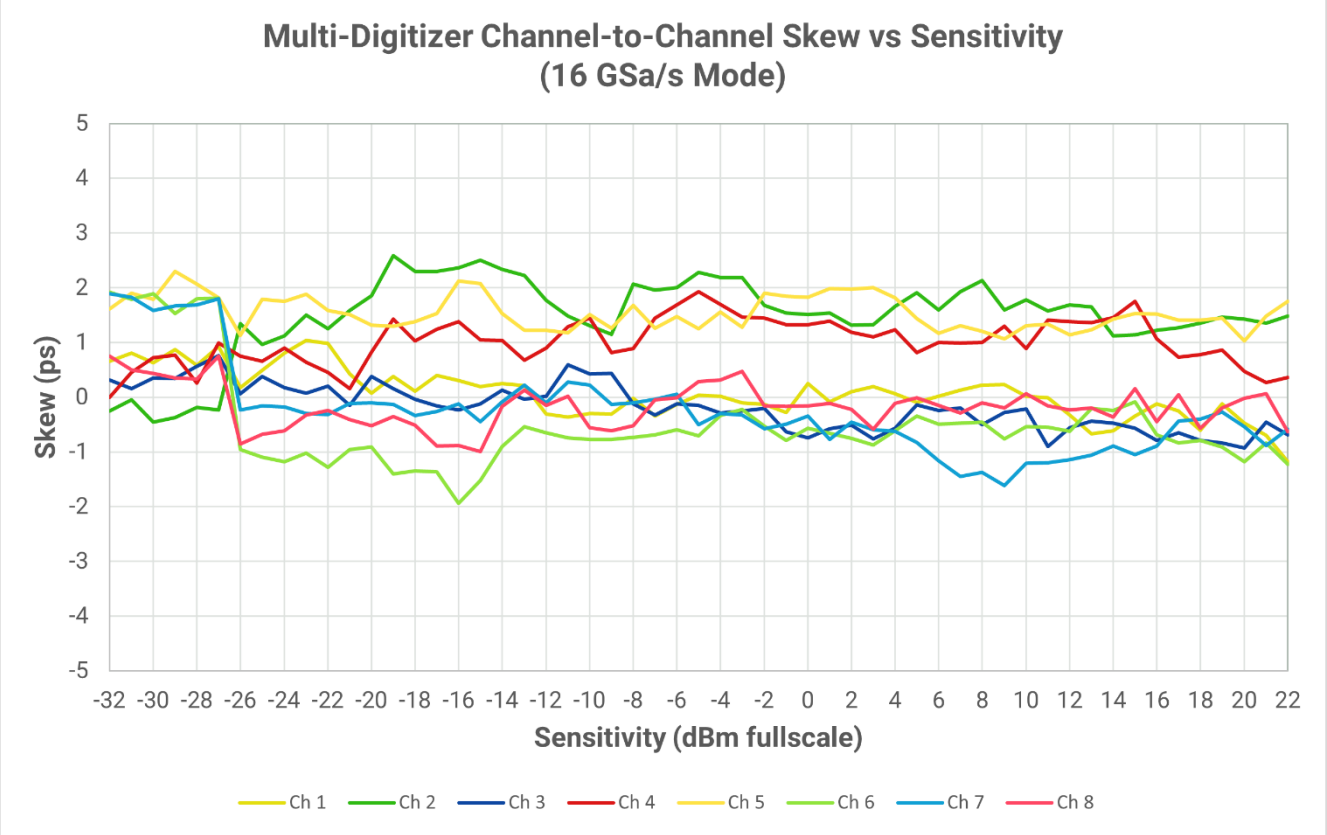

Figure 8. Multi-digitizer channel-to-channel skew vs sensitivity (16 GSa/s mode)

External Trigger

The external trigger (Trigger In) is converted to the digital domain and provides an accurate digitizer trigger with jitter < 1 ps. Additionally, the internal (channel) trigger can be used from any of the four analog input channels.

Clock Generator

The clock generator provides an 8 GHz clock for the ADC. This clock is multiplied inside the ADC to the sampling clock of 16 GHz or 32 GHz. The clock is generated from an internal OCXO generator and can be synchronized by a reference signal connected to Sync Clk In. The external reference signal must have a frequency stability equal to or better than ±2 ppm.

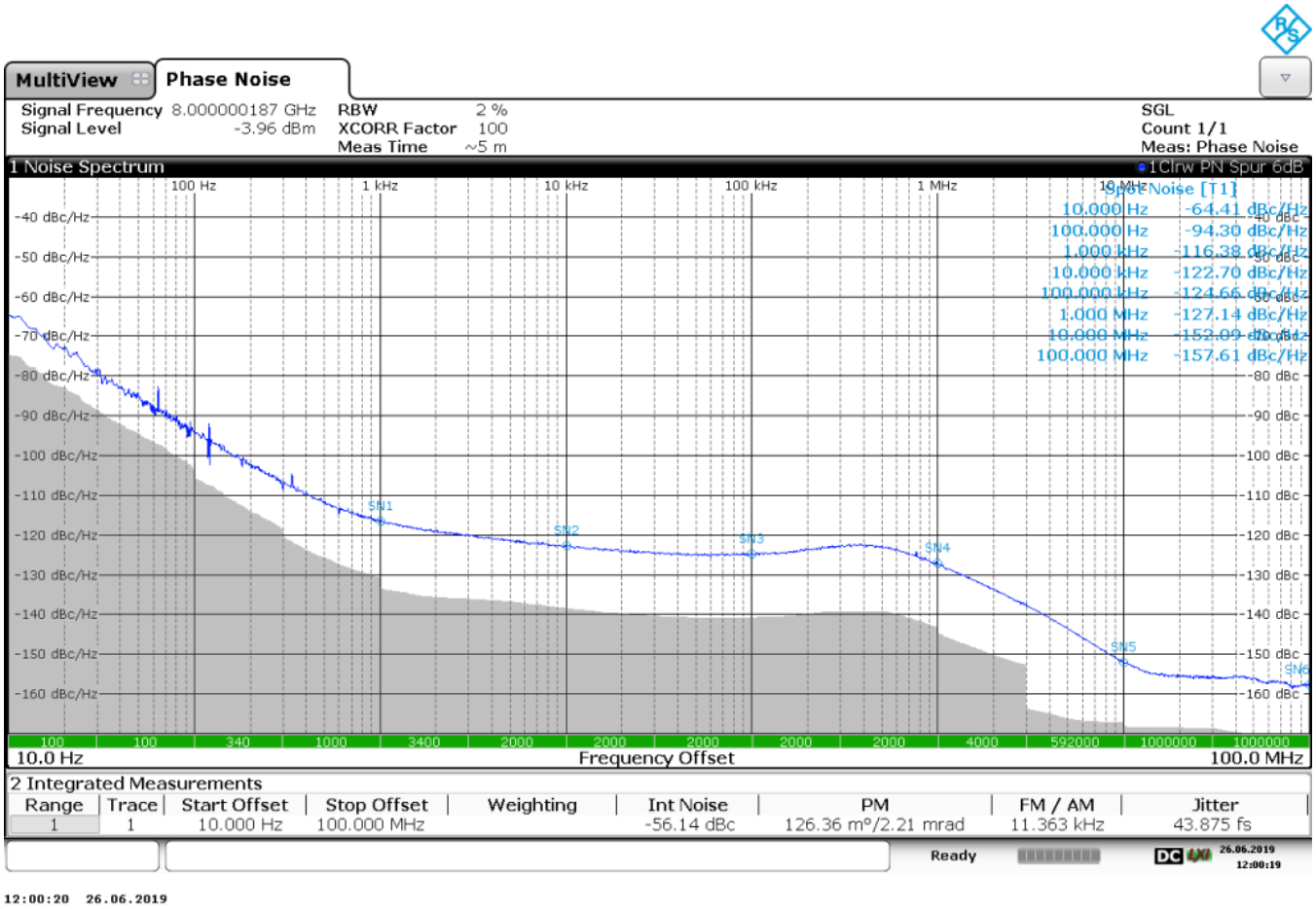

Figure 9. ADP7104 8 GHz clock phase noise (spur suppression mode)

FPGA Real-Time Processing

The data from the ADC is connected to FPGAs to perform real-time data processing. The FPGAs are each connected to its own 32 GB of memory per channel (64 GB with 256 GB memory option) used for data storage and processing. Additionally, acquired and processed data can be streamed to external devices through optical interfaces with throughput up to 80 GB/s.

Real-Time Equalization

Real-time equalization of amplitude frequency response and phase responses are performed for all channels. The equalization matches both responses to the target, a 6-pole Butterworth filter with linear phase response. The equalization is performed with input coax cables used to connect the digitizer's analog signal inputs, Ch 1, Ch 2, Ch 3 and Ch 4. Note, cable delays are matched with an accuracy < 1 ps to achieve required skew between channels.

Real-Time Low-Pass Filtering and Decimation

Real-time low-pass filtering with adjust bandwidth 10 GHz and down to 156.25 MHz (or 6.5 GHz and down to 101.5625 MHz for 16 GSa/s mode) and corresponding binary decimation from 1 to 64 can be performed for all channels. Filtering improves SNR and ENOB for low band signals. Additionally, filtering below 10 GHz (or 6.5 GHz) will result in data reduction, which requires less throughput to transfer the data to the host computer.

Real-Time Digital Down Converter (DDC)

Real-time digital down converter (DDC) with maximum span 2.5 GHz and decimation ratios 10 to 10 × 2^{16} (or 5 to 5 × 2^{16} for 16 GSa/s mode) can be performed for the four channels. The amplitude and phase frequency responses are equalized in real time to achieve accurate equalization in a narrow band of the DDC output signal. As a result, the DDC has an EVM = 0.471% with a real-time equalizer and software adaptive equalizer (in VSA software), see Figure 10.

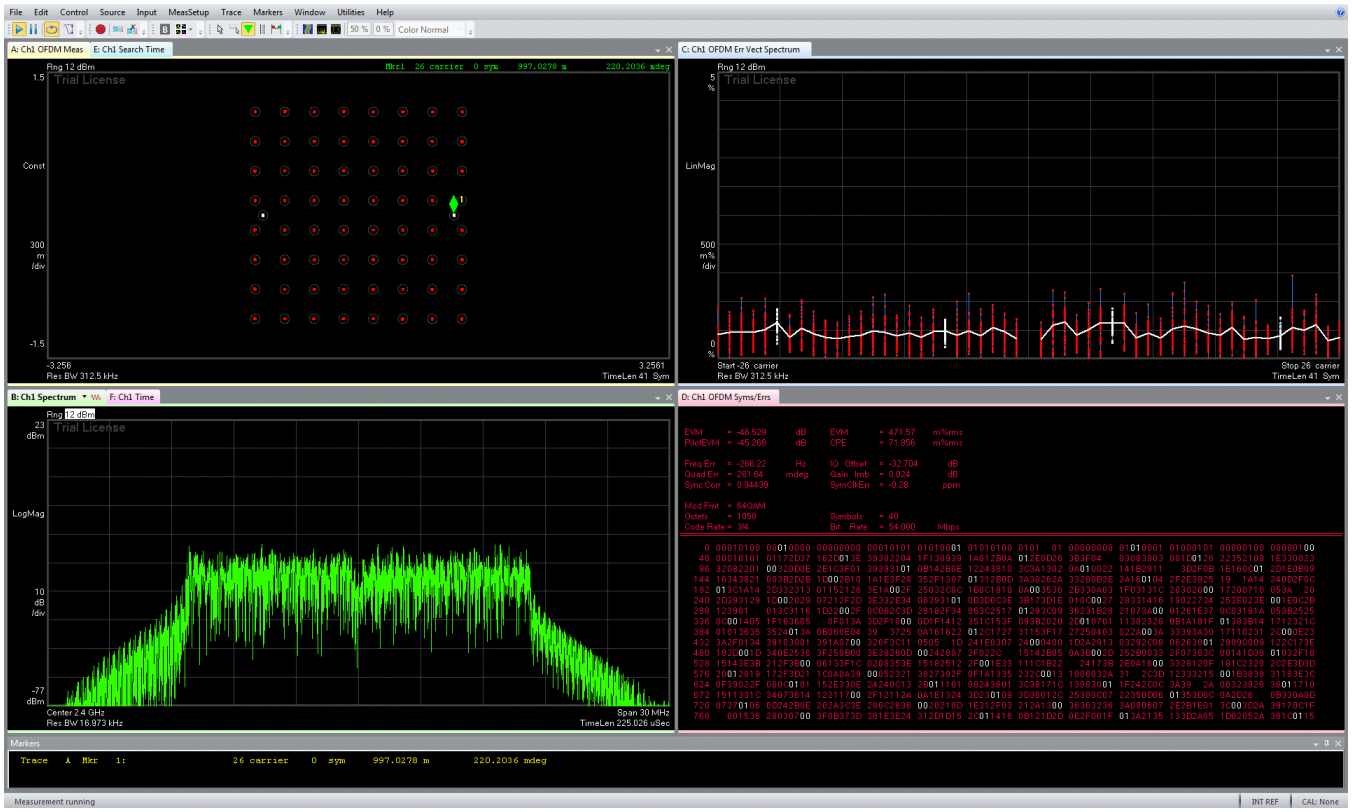

Figure 10. QAM64, 2.4 GHz center frequency, 30 MHz span

The I/Q signals skews between channels are adjusted. The skew between I/Q signals is measured in degrees. Figure 11 and Figure 12 shows the skew between the channels vs LO frequency for 32 GSa/s mode and 16 GSa/s mode, respectively. Figure 13 and Figure 14 shows the skew between channels vs sensitivity for 32 GSa/s mode and 16 GSa/s mode, respectively. The typical skew value is < ±10 degrees and < ±5 degrees for 32 GSa/s mode and 16 GSa/s mode, respectively.

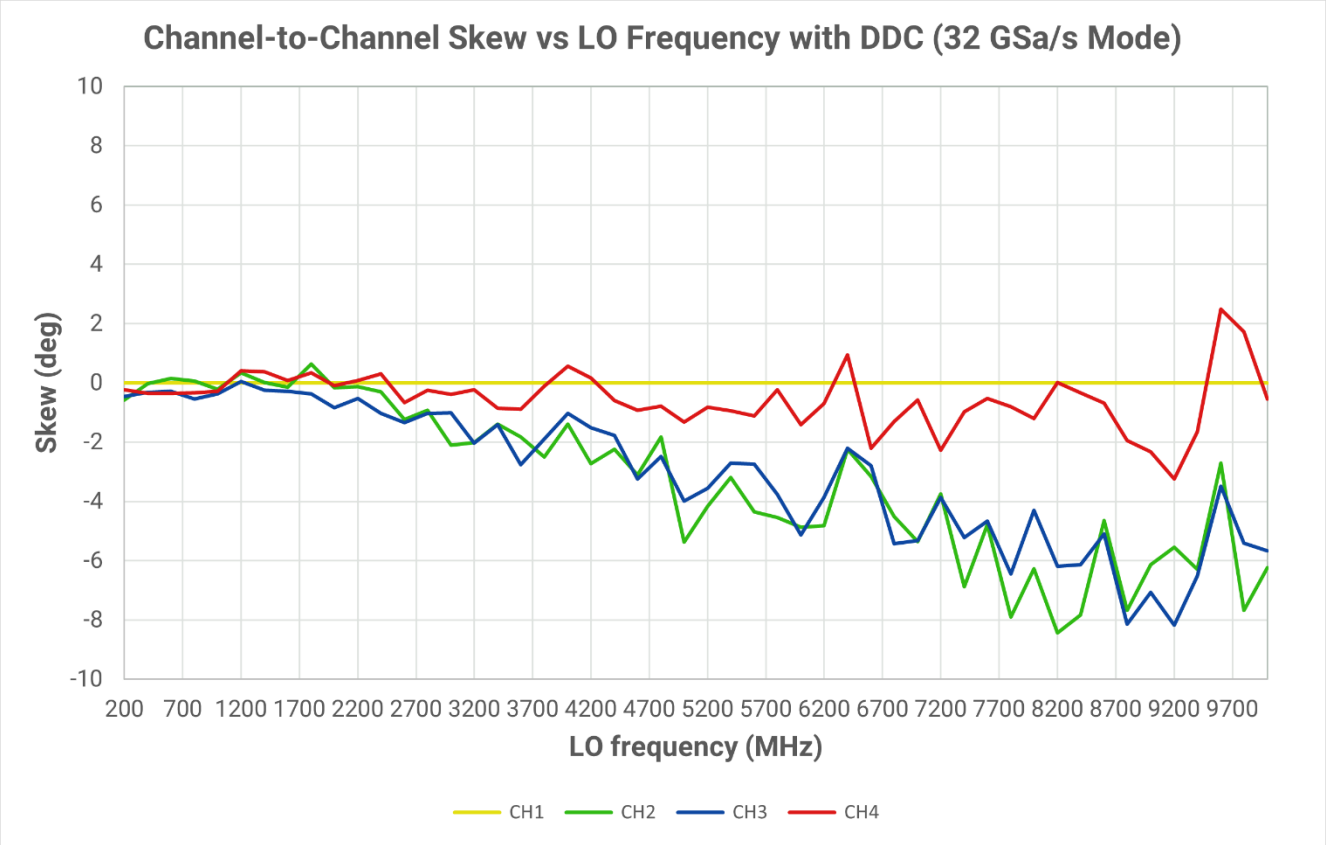

Figure 11. Channel-to-channel skew vs LO frequency with DDC (32 GSa/s mode)

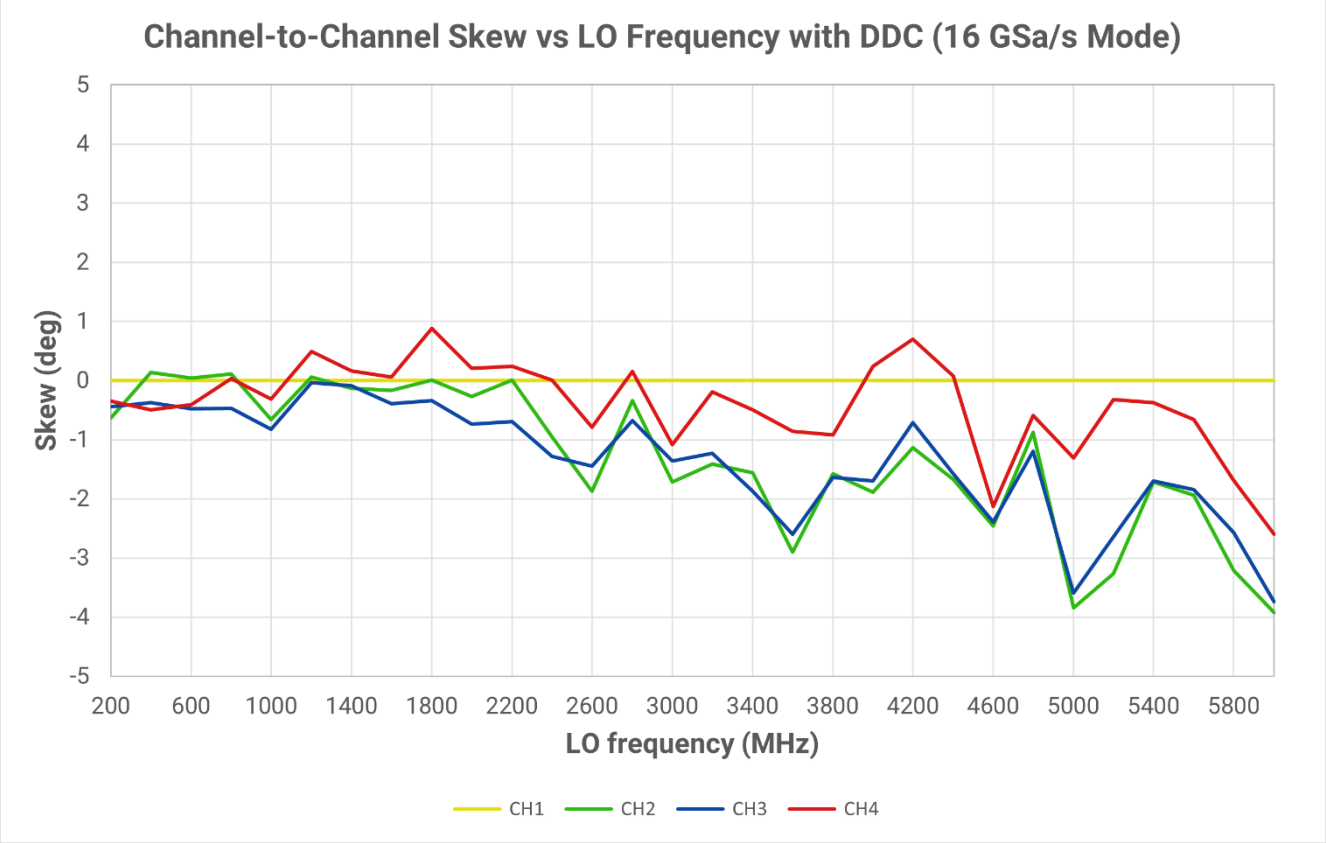

Figure 12. Channel-to-channel skew vs LO frequency with DDC (16 GSa/s mode)

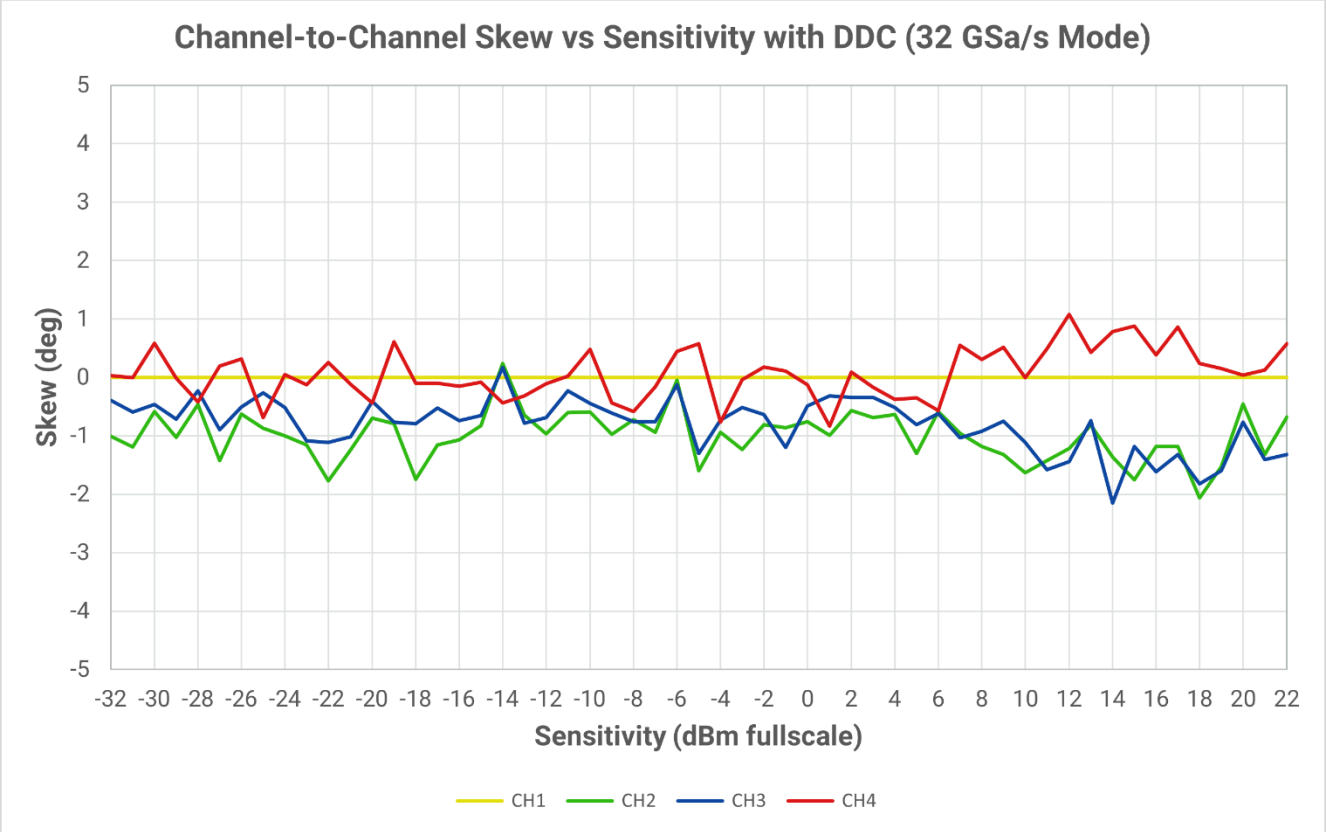

Figure 13. Channel-to-channel skew vs sensitivity with DDC (32 GSa/s mode)

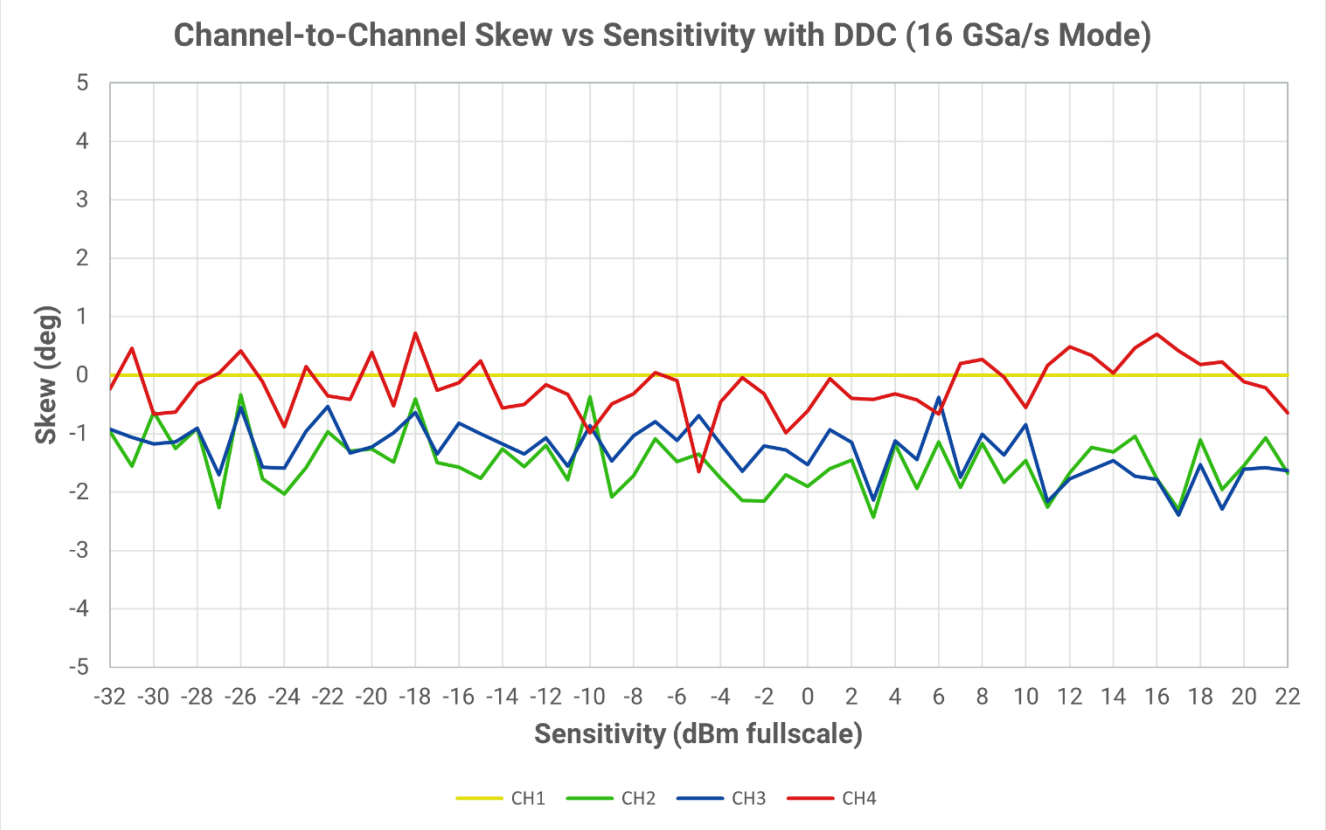

Figure 14. Channel-to-channel skew vs sensitivity with DDC (16 GSa/s mode)

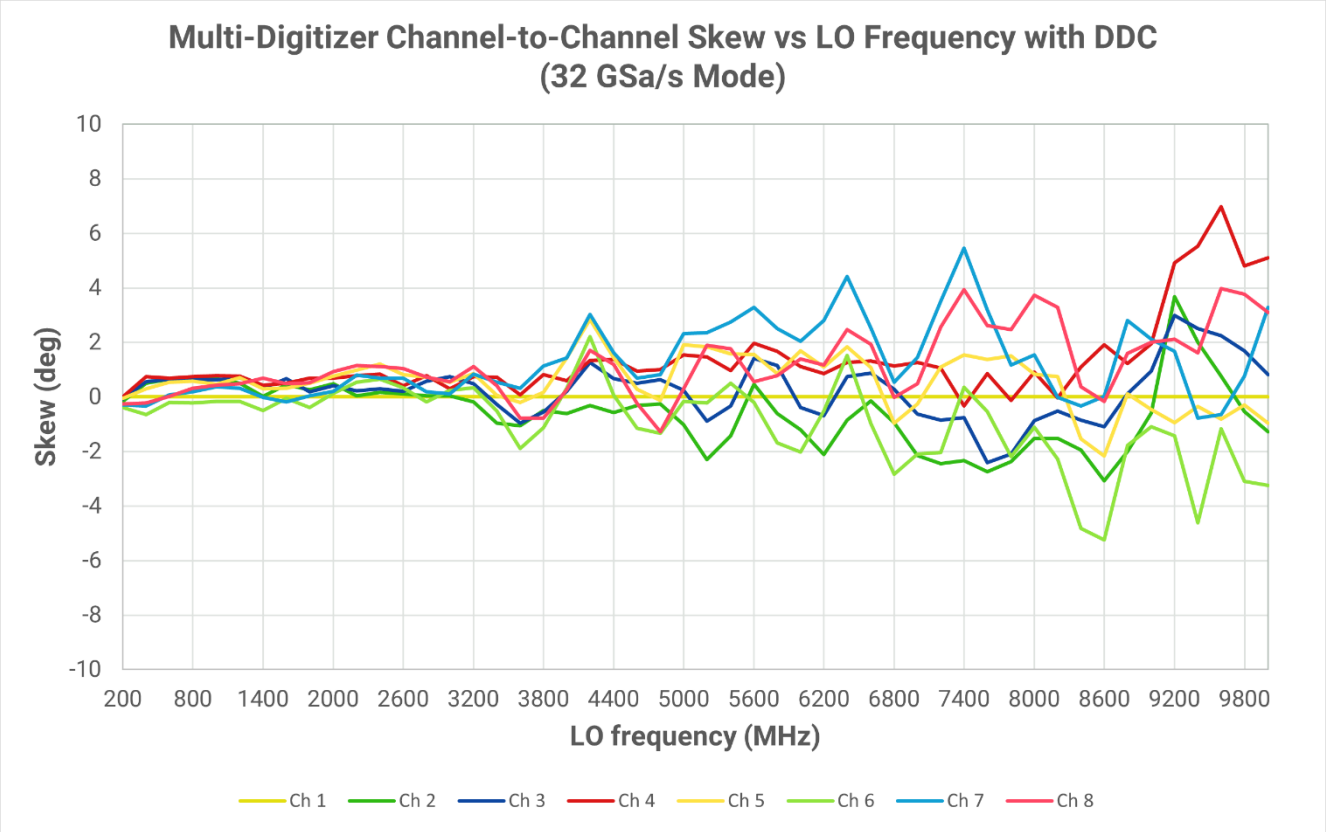

Figure 15. Multi-Digitizer Channel-to-channel skew vs LO frequency with DDC (32 GSa/s mode)

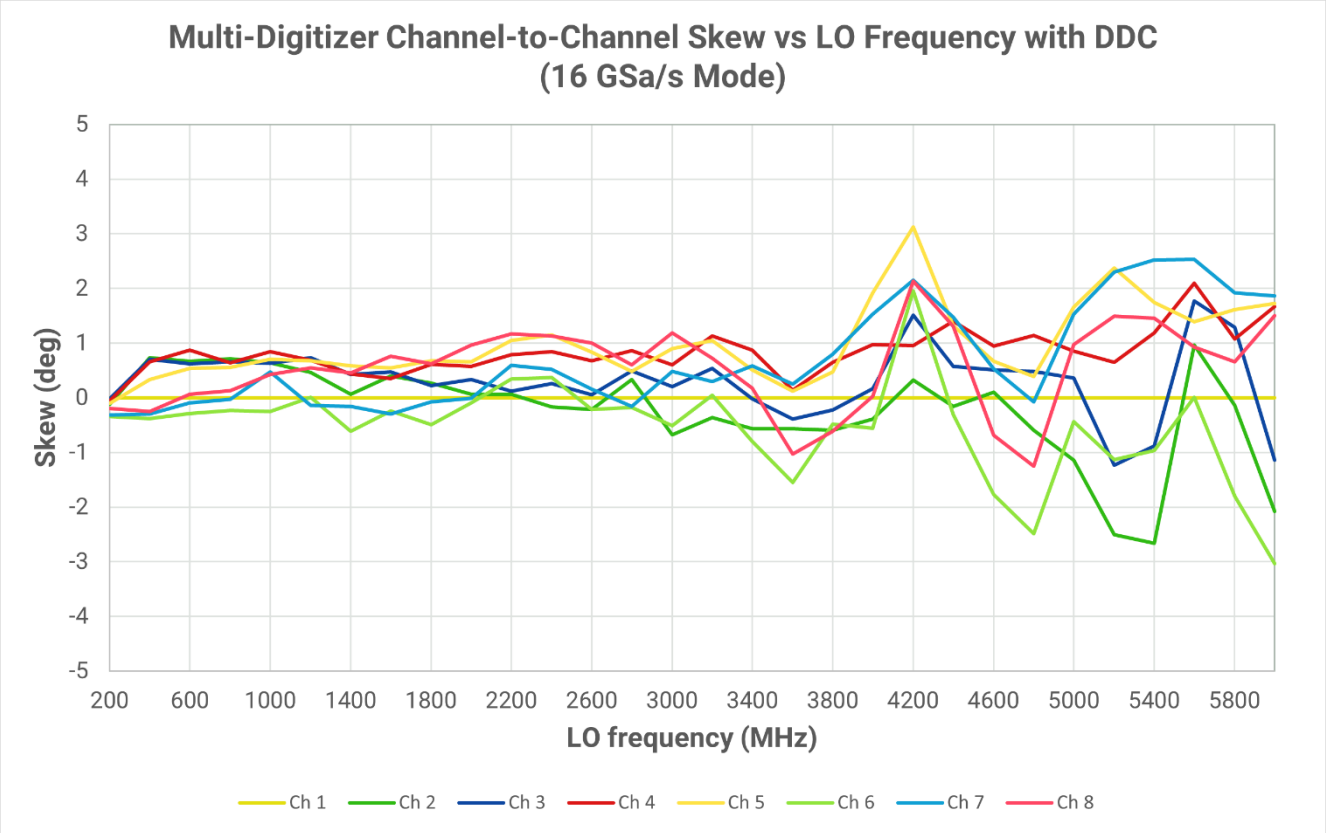

Figure 16. Multi-Digitizer Channel-to-channel skew vs LO frequency with DDC (16 GSa/s mode)

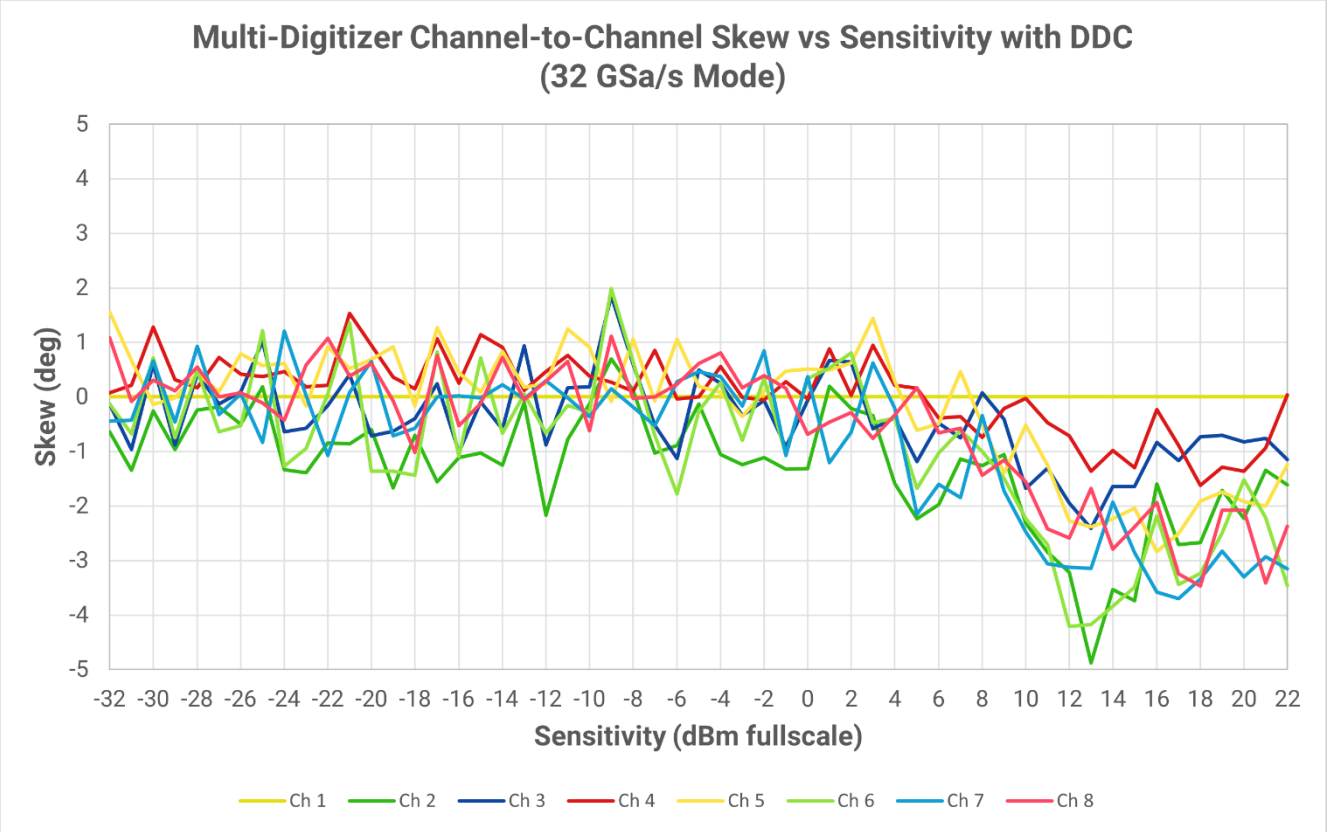

Figure 17. Multi-Digitizer Channel-to-channel skew vs sensitivity with DDC (32 GSa/s mode)

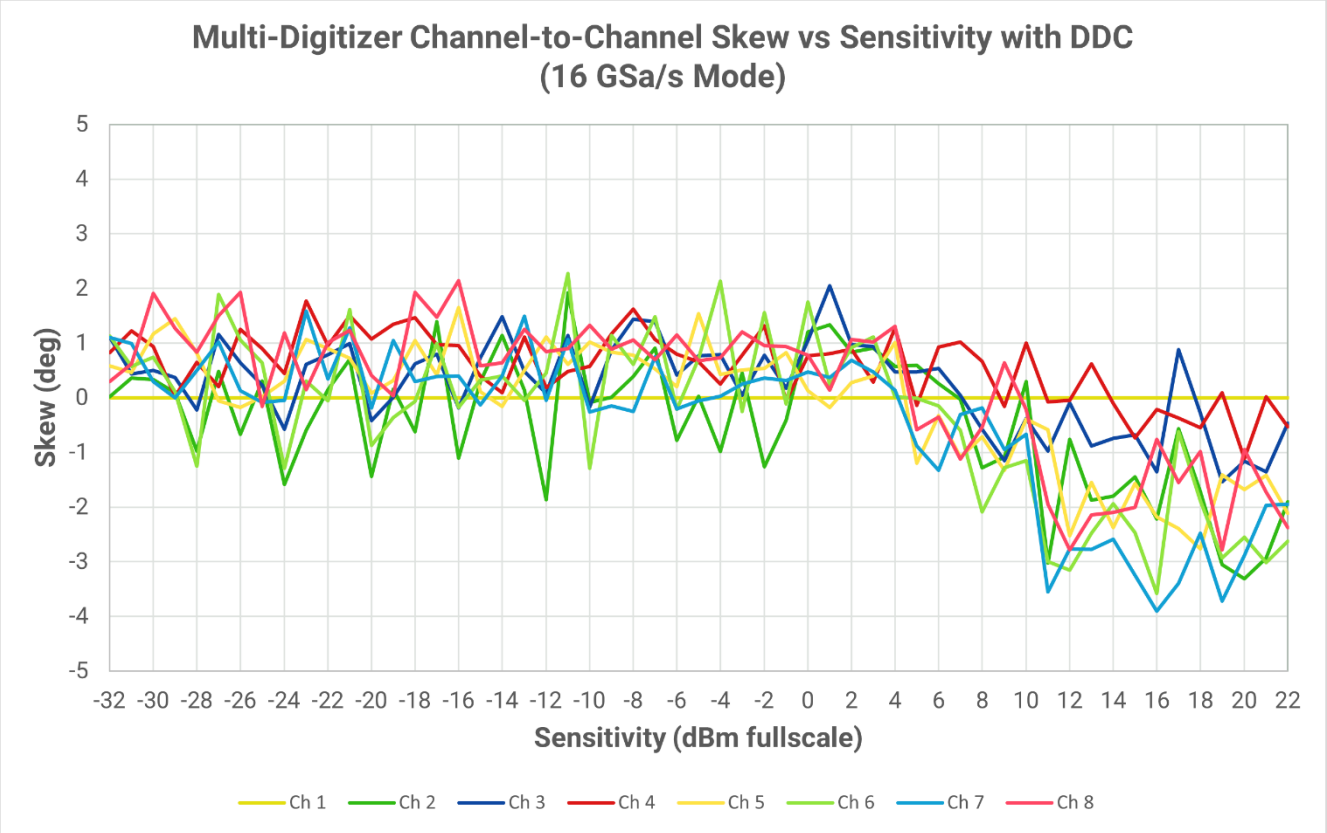

Figure 18. Multi-Digitizer Channel-to-channel skew vs sensitivity with DDC (16 GSa/s mode)

SDK and Command Line Utilities

Custom software applications can be written to control the ADP7104 using the GSA Software Development Kit (SDK). The SDK provides access to functions such as to initialize the hardware, acquire data, perform processing and transfer to host computer.

The GSA SDK API provides a set of functions exported from a Windows dynamic-link library (DLL). The API is declared in the C/C++ header (.h) file and alternatively in the type library (.tlb) file. The API can be used from C/C++ development environments such as Microsoft Visual C++ or National Instruments CVI by including the GSA SDK header file. This API can also be used with Microsoft .NET languages (C# and Visual Basic .NET) by referencing the GSA SDK type library. Additionally, the API can be used from the MATLAB language.

The GSA Toolkit includes several sample projects written in C++, C#, Visual Basic .NET and MATLAB. Several of these C++ sample projects are included in GSA Toolkit's installation as pre-compiled executable files. These projects can be used as a reference for customizing applications or to quickly and easily perform ADP7104 measurements.

Signal Display

Signal Display is a graphical application that controls the ADP7104 digitizer to observe input signals in time and frequency domains and perform acquisition of the signal. The software control panel has 4 display modes:

- Signal Display mode – to observe input signal in time domain (See Figure 19)
- Spectrum Display mode – to observe input signal in frequency domain (See Figure 20)
- DDC Display mode - to observe down converted signal in time domain (See Figure 21)
- DDC Spectrum Display mode - to observe down converted signal in frequency domain (See Figure 22)

Signal Display is also used to control multiple synchronized digitizers.

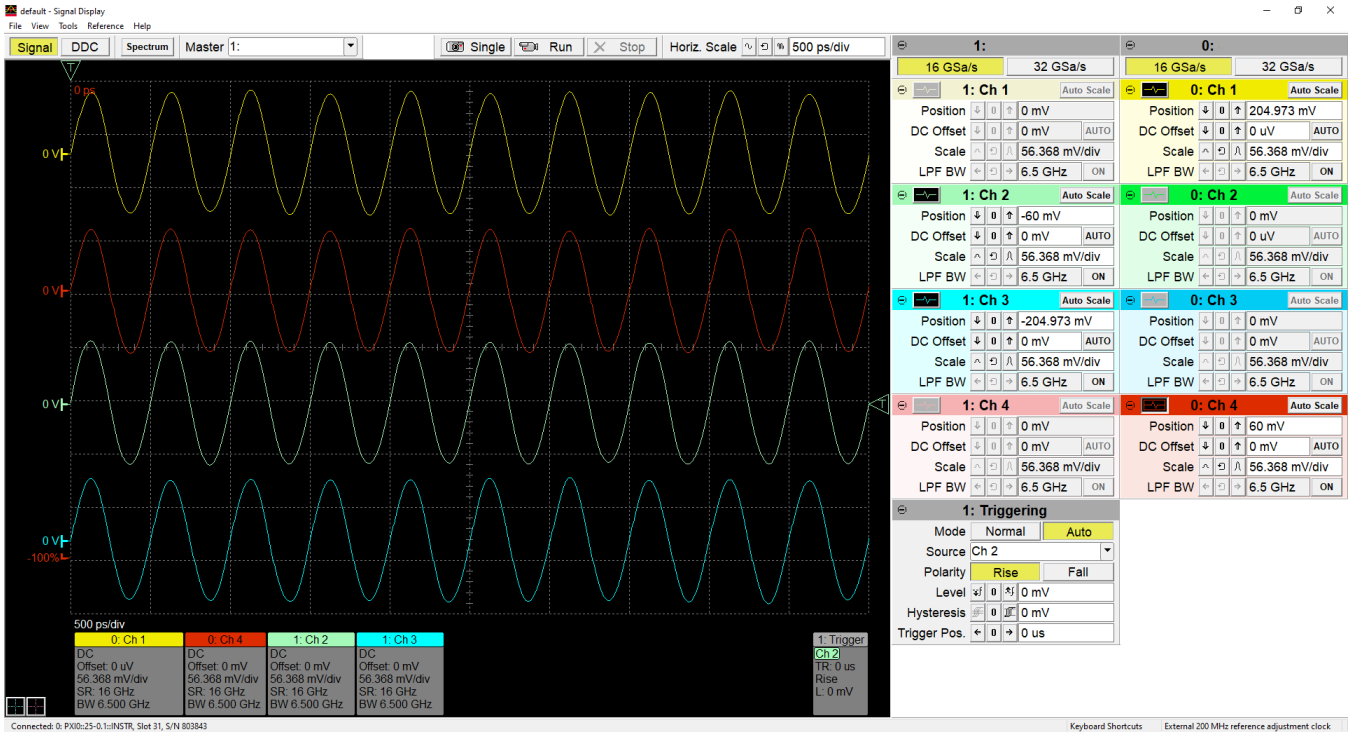

Figure 19. Signal (time domain) display with software control panel

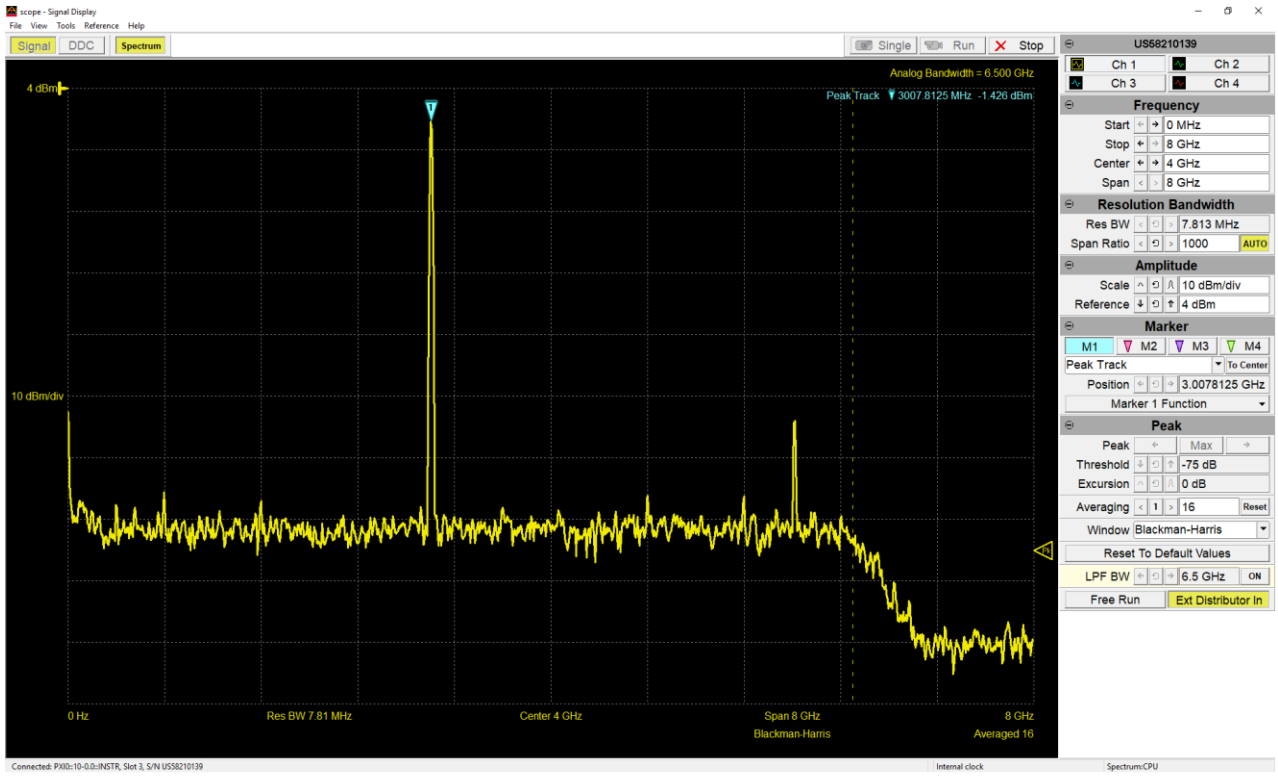

Figure 20. Spectrum analyzer (frequency domain) display with software control panel

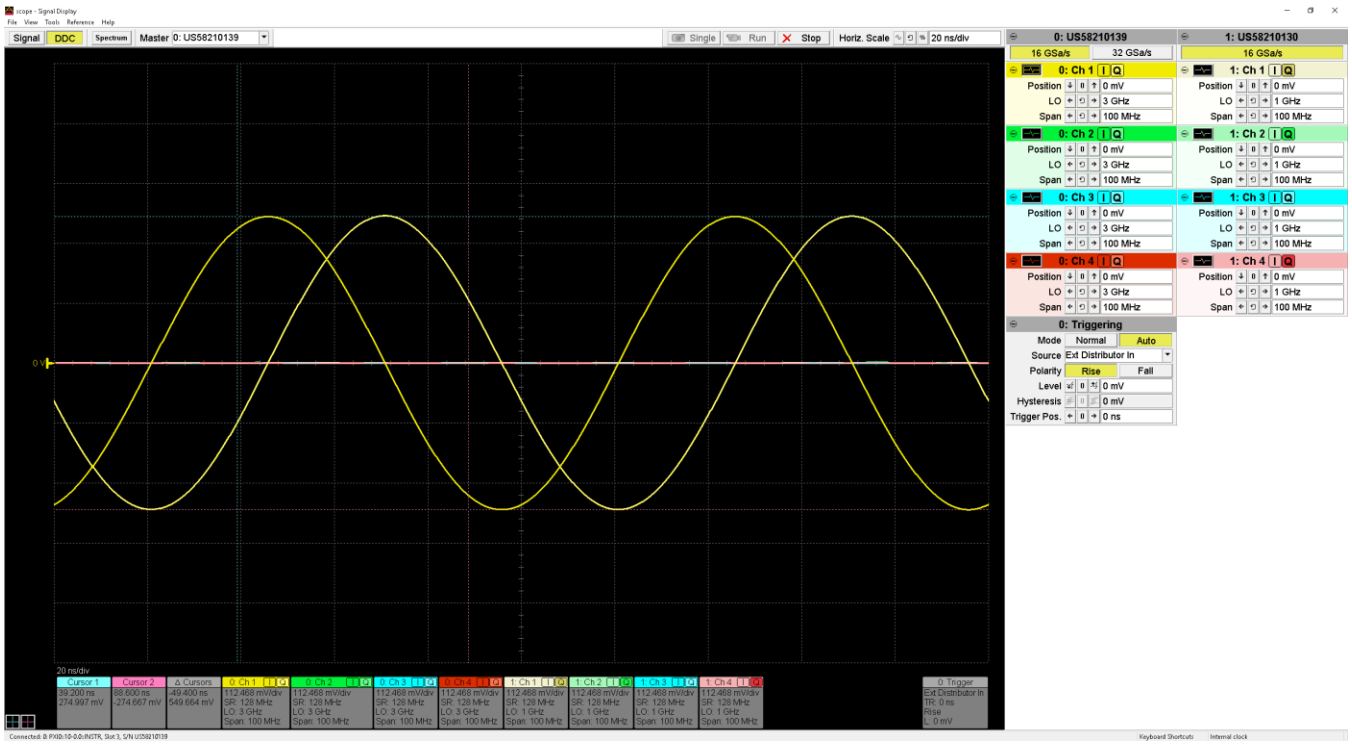

Figure 21. DDC signal (time domain) display with software control panel

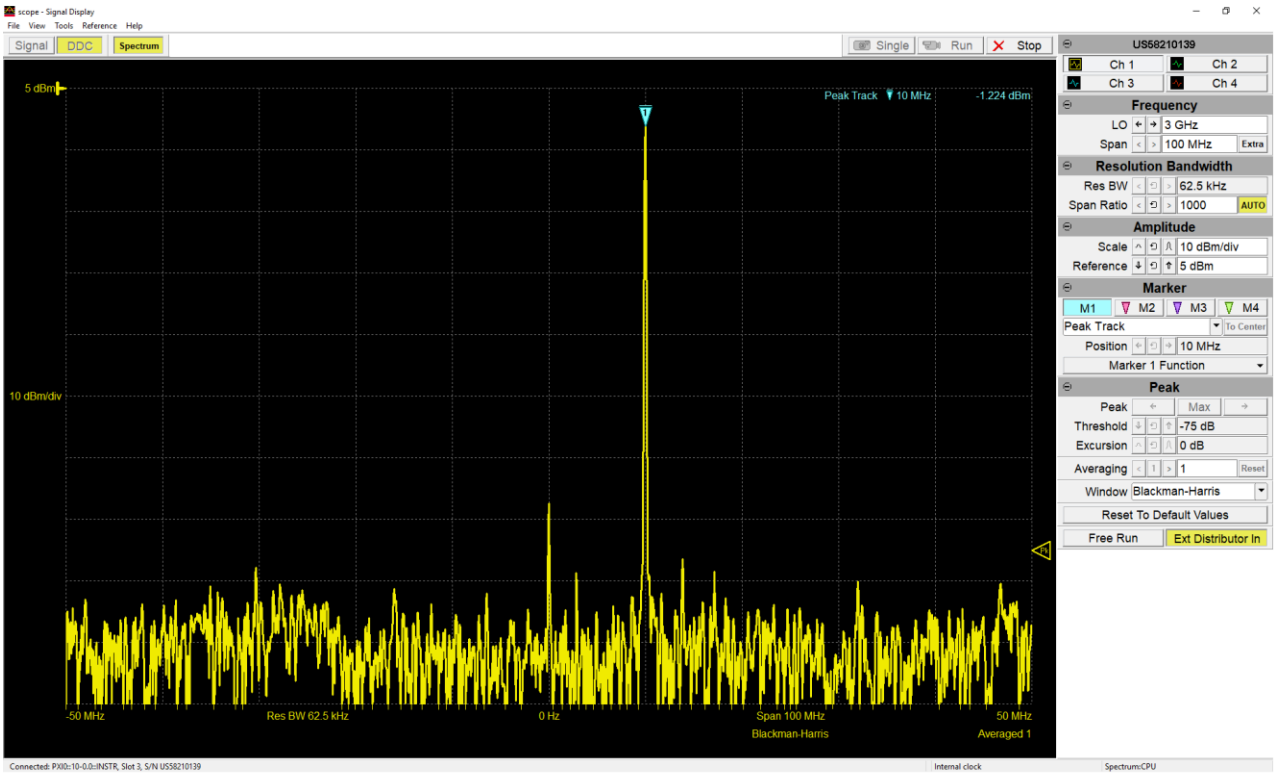

Figure 22. DDC spectrum analyzer (frequency domain) display with software control panel

Specification

Vertical System

	2 Channel Mode – 32 GSa/s	4 Channel Mode – 16 GSa/s
Number of channels	2	4
Input connector type	SMA	
Maximum sampling rate	32 GSa/s	16 GSa/s
Analog bandwidth (-3 dB)[1,2]	DC … 10 GHz	DC … 6.5 GHz
Bandwidth flatness (-6 dBFS)[1]	±0.5 dB to 8.5 GHz	±0.5 dB to 5 GHz
Vertical resolution	10 bits	
Input impedance	50 Ω ± 3.5% (typical ±1% at 25 ºC)	
Return loss	16 dB @ 0 … 9 GHz (< 320 mV) 19 dB @ 0 … 9 GHz (> 320 mV) 12 dB @ 10 GHz (< 320 mV) 13 dB @ 10 GHz (> 320 mV)	16 dB @ 0 … 9 GHz (< 320 mV) 19 dB @ 0 … 9 GHz (> 320 mV) 12 dB @ 10 GHz (< 320 mV) 13 dB @ 10 GHz (> 320 mV)
Input coupling	DC	
Maximum input voltage	±5 V	
Input sensitivity	16 mV_{pp} … 8 V_{pp} (full scale) (-32 dBm … +22 dBm with 1 dB calibrated sensitivities)	
Phase response[1]	±2 deg	±1 deg
Effective number of bits (ENOB)[1,3] (-3 dBFS, 400 mV full scale)	6.2	6.5
Rise / fall time (20 - 80%, measured)	29 ps	45 ps
Rise / fall time (10 - 90%, measured)	39 ps	64 ps
RMS Noise Floor[1]	375 uV @ 16 mV full scale 384 uV @ 40 mV full scale 448 uV @ 80 mV full scale 553 uV @ 160 mV full scale 1.492 mV @ 400 mV full scale 3.07 mV @ 800 mV full scale 5.9 mV @ 1.6 V full scale 13.802 mV @ 4 V full scale 23.279 dB @ 8 V full scale	236 uV @ 16 mV full scale 254 uV @ 40 mV full scale 315 uV @ 80 mV full scale 396 uV @ 160 mV full scale 1.198 mV @ 400 mV full scale 2.437 mV @ 800 mV full scale 4.94 mV @ 1.6 V full scale 11.266 mV @ 4 V full scale 20.149 mV @ 8 V full scale
Spurious Free Dynamic Range (SFDR)[1] (-3 dBFS, 400 mV full scale) (excluding in-band 2nd and 3rd harmonics)	> 70.1 dBc @ 1 GHz	> 68.1 dBc @ 1 GHz

Nonlinear distortions HD2 (-3 dBFS, 400 mV full scale)	> 58 dBc @ 2 GHz > 48 dBc @ 4 GHz	> 56 dBc @ 2 GHz > 54 dBc @ 3 GHz
Nonlinear distortions HD3 (-3 dBFS, 400 mV full scale)	> 52 dBc @ 2 GHz > 50 dBc @ 3 GHz	> 55 dBc @ 1 GHz > 51.8 dBc @ 2 GHz
Channel-to-channel skew (for all sensitivities, see Figure 4, Figure 5)	< ±2 ps	
Multi-digitizer channel-to-channel skew (for all sensitivities, see Figure 7, Figure 8)	< ±5 ps	
Channel-to-channel isolation (any two channels with equal sensitivity)	72 dB @ 100 MHz … 1 GHz 49 dB @ > 1 GHz	
DC Gain accuracy	±3% of full scale at full resolution (±1% for 40 mV to 8 V full scale)	
Offset range (for all sensitivities)	±4.5 V	

Acquisition System

	2 Channel Mode – 32 GSa/s	4 Channel Mode – 16 GSa/s
Sampling rate (per channel)	32 GSa/s	16 GSa/s
Single sideband (SSB) phase noise (8 GHz clock to ADC)	< -116 dBc/Hz (typical) at 1 kHz offset	
8 GHz clock to ADC jitter (10 Hz – 10 MHz)	< 43.9 fs	
Memory depth	128 GB (upgradable to 256 GB memory option)	
Maximum acquisition time (per channel at maximum sampling rate)	1.71 s (typical) 3.43 s (typical with 256 GB memory option)	

Data Transfer Throughput Speed to Computer

Form factor	Guzik enclosure	2-slot AXIe
Optical Data Interface	Up to 10 GB/s	
PCI Express Gen 3 x8	Up to 5 GB/s	Not available
PCI Express Gen 2 x4	Up to 1.25 GB/s	

Real-Time Digital Down-Converter

Maximum span	2.5 GHz
DDC results data format	I (16-bit) and Q (16-bit)
Frequency response flatness	±0.2 dB
Out of band attenuation (max span)	> 50 dB
EVM (30 MHz span, QAM 64, with adaptive VSA equalizer)	< 0.471%
Channel skew (I/Q skew between channels) for different LO frequencies (see Figure 11)	< ±10 deg (32 GSa/s mode) < ±5 deg (16 GSa/s mode)
Channel skew (I/Q skew between channels) for different sensitivities (see Figure 13)	< ±3 deg (32 GSa/s mode) < ±3 deg (16 GSa/s mode)
Channel trigger types	Magnitude
Decimation ratio	10 … 10 × 2^{16} (32 GSa/s mode) 5 … 5 × 2^{16} (16 GSa/s mode)

Real-Time Averaging

ADC resolution	10 bits
Averaged resolution	64 bits
Number of averages	> 50 million (with 256 GB memory option)
Trigger jitter	< 1 ps RMS
Maximum trigger pulse rate	2 MHz 25 MHz (with upgradable option)
Trigger rearm time	390 ns 25 ns (with upgradable option)
Averaging window	20 us (maximum) 110 ns (minimum)
Trigger utilization	≥ 99%
Pre-trigger range	0 … 4.5 us in 5 ns increments
Post-trigger range	0 … 21 s in 5 ns increments
Trigger-to-data alignment accuracy	≤ 10 ps
Classifying markers	Up to 8

Internal Time Base

Frequency	1 GHz (nominal)
Time base accuracy	±50 ppb stability (v. Temperature 0ºC to 50ºC) + aging aging < ±2 ppm/10 years (maximum) aging < ±0.3 ppm/first year (typical) aging < ±5 ppb/day (typical)
Single sideband (SSB) phase noise	< -145 dBc/Hz (typical) at 10 kHz offset

Channel Digital Trigger

Edge trigger	Rising or falling edge
Frequency range	0 … 10 GHz (32 GSa/s mode) 0 … 6.5 GHz (16 GSa/s mode)
Rearm time (deadtime)	196 ns
Max trigger frequency (100% trigger utilization)	3.5 MHz
Threshold adjustment	Full scale
Threshold resolution	12 bit
Pre-trigger range	1.7 s (typical)
Post-trigger range	5.3 s (typical)
Hold-off time	21.4 s (typical)

External Trigger (Aux Trigger In)

Edge trigger	Rising or falling edge
Rearm time (deadtime)	196 ns
Max trigger frequency (100% trigger utilization, pre-trigger < 300 ns)	3.5 MHz
Pre-trigger range	1.7 s (typical)
Post-trigger range	5.3 s (typical)
Hold-off time	21.4 s (typical)
Trigger jitter	< 1 ps RMS
Front panel connector	1 MCX female
Impedance	50 Ω
Coupling	DC
Input range	±2.5 V
Trigger threshold range	±2.5 V
Threshold resolution	0.1 mV (nominal)
Minimum pulse width	150 ps TBD

Frequency range	up to 4 GHz, 210 MHz without pulses skipping
Hysteresis	10 mV (typical)
Sensitivity	100 mV at max frequency (30 mV at 10 MHz)
Slew rate	≥ 4 V/ns for best jitter performance

Trigger Output (Aux Trigger Out)

Front panel connector	1 MCX female
Impedance	50 Ω
Common mode voltage	-200 mV
Level	CML, 400 mV_{pp}
Coupling	DC
Rise / Fall Time (20 - 80%)	120 ps
Delay to trigger input	3 ns (typical)
Slew rate	≥ 4 V/ns

Trigger Distributor In

Front panel connector	1 MCX female
Impedance	50 Ω
Level	±2.5 V
Coupling	DC
Slew rate	≥ 4 V/ns for best jitter performance

Trigger Distributor Out

Front panel connector	6 MCX female
Impedance	50 Ω
Level	0.4 V_{pp} (nominal)
Common mode	0 V
Coupling	DC
Slew rate	≥ 4 V/ns

1 GHz Reference Clock In (1 GHz In)

Front panel connector	1 MCX female
Impedance	50 Ω
Level	0 … +10 dBm
Coupling	AC
Lock range	±2 ppm (maximum)
Slew rate	≥ 4 V/ns for best jitter performance

1 GHz Reference Clock Out (1 GHz Out)

Front panel connector	1 MCX female
Impedance	50 Ω
Frequency	1 GHz
Level	400 mV_{pp} (nominal)
Coupling	AC
Time base accuracy	±50 ppb stability (v. Temperature 0ºC to 50ºC) + aging aging < ±2 ppm/10 years (maximum) aging < ±0.3 ppm/first year (typical) aging < ±5 ppb/day (typical)
SSB phase noise	< -145 dBc/Hz (typical) at 10 kHz offset
Slew rate	≥ 4 V/ns

Reference Clock Input (Sync Clk In)

Front panel connector	1 MCX female
Impedance	50 Ω
Frequency	31.25 kHz … 500 MHz (multiples of 2)
Level	+2 dBm … +10 dBm
Coupling	AC
Slew rate	≥ 4 V/ns for best jitter performance
Lock range	±2 ppm (maximum)

Reference Clock Output (Sync Clk Out)

Front panel connector	1 MCX female
Impedance	50 Ohm
Frequency	200 MHz
Level	400 mV_{pp} (nominal)
Coupling	AC
Slew rate	≥ 4 V/ns

Test Out (Test Out)

Front panel connector	4 MCX female
Impedance	50 Ω
Level	3.3 V LV TTL

Clock Distributor In (Sync Clk Distributor In)

Front panel connector	1 MCX female
Impedance	50 Ω
Level	0.4 … 3 V_{pp}
Coupling	AC
Slew rate	≥ 4 V/ns for best jitter performance

Clock Distributor Out (Sync Clk Distributor Out)

Front panel connector	6 MCX female
Impedance	50 Ω
Level	0.4 V_{pp} (nominal)
Coupling	AC
Slew rate	≥ 4 V/ns

Gate Input

Front panel connector	4 MCX female
Impedance	50 Ω
Input range	±2.5 V
Coupling	DC
Minimum pulse width (100% utilization)	5 ns
Threshold range	±2.5 V
Hold-off time	300 ns (post-trigger mode) 350 ns (pre-trigger mode)

ODI Port

Front panel connector	4 MPO/MTP 24 Fiber connector
Class I laser	85 nm VCSEL
Function	Data transfer
Throughput (per port)	Up to 20 GB/s

ODI Ctrl

Front panel connector	1 MPO/MTP 24 Fiber connector
Class I laser	85 nm VCSEL
Function	Data transfer and digitizer control
Throughput	Up to 10 GB/s

Spare

Front panel connector	1 MCX Female

I/O External

I/O External (IO Ext)	1 Samtec ERF8-020

Host Computer

Form factor	Guzik enclosure	2-slot AXIe
Transfer Interface	Optical Data Interface PCI Express Gen 3 x8 or Gen 2 x4	PCI Express Gen 2 x4
Operating System	64-bit Windows 10 64-bit Windows 7	

General Specifications

Form factor	Guzik enclosure	2-slot AXIe
Chassis	Not applicable	Requires compatible chassis
Dimensions (width x height x depth)	482.6 x 71.12 x 514.35 mm 19 x 2.8 x 20.25 inches	322.5 x 60 x 281.5 mm 12.7 x 2.36 x 11.1 inches (excludes chassis)
Weight	10.43 kg 23 lb	5 kg (excludes chassis) 11 lb (excludes chassis)
Power dissipation	400 W maximum	
RoHS	EU/2015/863	
Operating temperature range	+5°C to +40°C	
Non-operating temperature	-40°C to +70°C	
Operating humidity	5% to 80% relative humidity, non-condensing	
Operating altitude	Up to 4,000 meters (12,000 feet)	
Non-operating altitude	Up to 15,300 meters (50,000 feet)	
Calibration interval	1 year recommended	

Ordering Information

Part Number	Description
S90-620205-02	ADP7104 Digitizer in Guzik Enclosure with PCIe Gen3 x8 Interface
S90-620205-02.04	ADP7104 Digitizer in Guzik Enclosure with PCIe Gen2 x4 Interface
S90-620205-02.04.B1	ADP7104 Digitizer in Guzik Enclosure with PCIe Gen2 x4 Interface and ADC_AVGA: Real-Time Signal Averaging software option license

[1] With digital equalization
[2] 6-pole Butterworth approximation
[3] ENOB is calculated as the following:

$$\text{ENOB} = \frac{\text{SINAD}_{\text{MEASURED}} - 1.76\ \text{dB} + 20 \log\left(\frac{\text{Fullscale Amplitude}}{\text{Input Amplitude}}\right)}{6.02}$$

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02-107761-02
05/24/2024