Digital Down-Converter with Baseband Mismatch Equalization

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Our recent paper [1] described different approaches to digital real-time signal equalization for Time-Interleaved ADCs (TIADC). When equalization is applied before down-conversion, mismatch of ADCs slices can be corrected, however real-time implementation is not feasible – it requires large number of multipliers operating at full ADC sampling rate. Equalization of down-converted signal can be implemented in real-time. It operates at lower sampling rate and does not require large number of Finite Impulse Response (FIR) filter taps; however, this method cannot correct mismatches of ADC slices.

Real-Time DDC method described in [1] operates at down-converted sampling rate and achieves real-time performance. However, it requires large number of FIR equalizer taps which is difficult to achieve due to limited number of available multipliers. Implementation of this method in Guzik ADP7000 series digitizers has 160 FIR equalizer taps. As shown in [2], longer equalizer response (e.g. 500-800 taps) may be required for accurate equalization of RF components.

An innovative solution to the problem of base-band down conversion with ADC slice equalization is described in recent U.S. Patent [3], issued to Guzik Technical Enterprises in May 2019.

Figure 1 depicts block-diagram of the new digital downconverter with baseband equalization. Composite ADC consists of M sub-ADCs. Each individual sub-ADC with the number m ($0 \le m \le M - 1$) have a frequency response $H_m(f)$. Due to the imperfection of the analog part of each sub-ADC, the frequency responses $H_m(f)$ are distorted and are different for different m.

The enclosed equalization method is based on processing of sub-ADC output samples using individual IQ demodulators. IQ demodulator is equivalent to standard down-converter mixer with Local Oscillator (LO) center frequency, low pass filtering and decimation. Outputs of IQ demodulators represent under-sampled in-phase and quadrature samples produced by individual sub-ADCs.

These samples are processed by misalignment equalizers – complex FIR filters which eliminate mismatch of sub-ADC frequency responses. All in-phase and quadrature samples are combined in Adders 0 and 1, forming “pre-I” and “pre-Q” samples. These samples are filtered in “Common Equalizer”, correcting frequency distortions, common for all ADC slices and providing desired target frequency response of output I and Q samples.

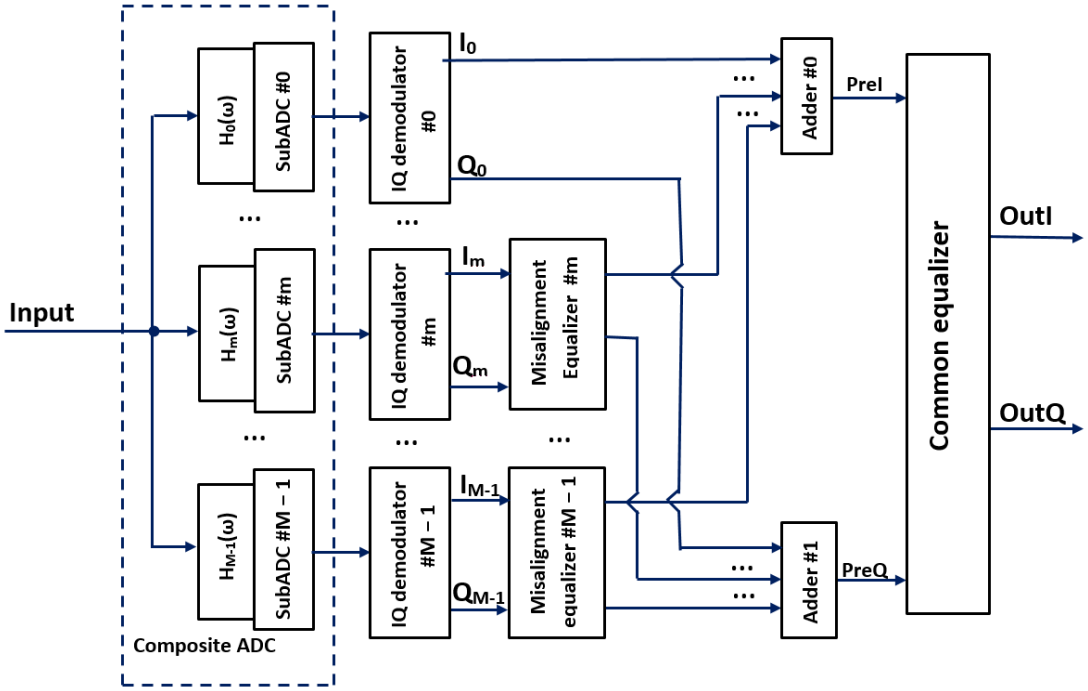

Figure 1 Block-diagram of digital down-converter with baseband equalization

The baseband equalization system shown in Figure 1 is feasible for modern ADC chips having relatively small number of ADC slices. Recent advances in interleaved ADCs combine multiple ADC slices within the single silicon structure and allow high quality calibration and alignment of sub-ADC amplitude and phase responses. Typically, high speed ADCs (for example Keysight 10-bit 32 GS/s ADC) consists of two sub-ADCs (quadrants), each operating at 16 GS/s. Individual sub-ADC slices within each quadrants can be calibrated to minimize amplitude and frequency deviations. However, resulting slice misalignment between two quadrants cannot be removed, therefore this 32 GS/s composite ADC can be effectively described as only 2 slice structure. Similarly, 64 GS/s ADC system consisting of 4 quadrants can be represented as having 4 ADC slices.

Since each sub-ADC operates with under-sampling, the signal at its output contains aliasing frequency components reflected from the frequencies $k \cdot f_s/M$, $1 \le k \le M - 1$. This results in complicated signal spectrum, combining useful and distorted signal components. As shown in [3], proper choice of misalignment equalizers will eliminate distorted spectral components. The frequency responses of misalignment equalizers are found by solving system of equations, based on sub-ADC frequency responses and phases of ADC slices.

In practice, misalignment equalizers have small number of FIR taps correcting inter-slice frequency responses. Figure 2a shows amplitude and phase deviations between two slices of Guzik ADP7000 digitizer, with maximum amplitude deviation of 1% and phase deviation of 0.015 rad. While these amplitude and phase misalignments are small, they may still cause about 0.5 % Error Vector Magnitude (EVM) degradation. Note that slice deviations are smooth functions of

frequency. Impulse response of "inter-slice" frequency response is shown in Figure 2b and is concentrated within 2 ns time interval. Only 7 FIR taps were sufficient for compensating this response using 32 GS/s ADC and decimation factor of 10.

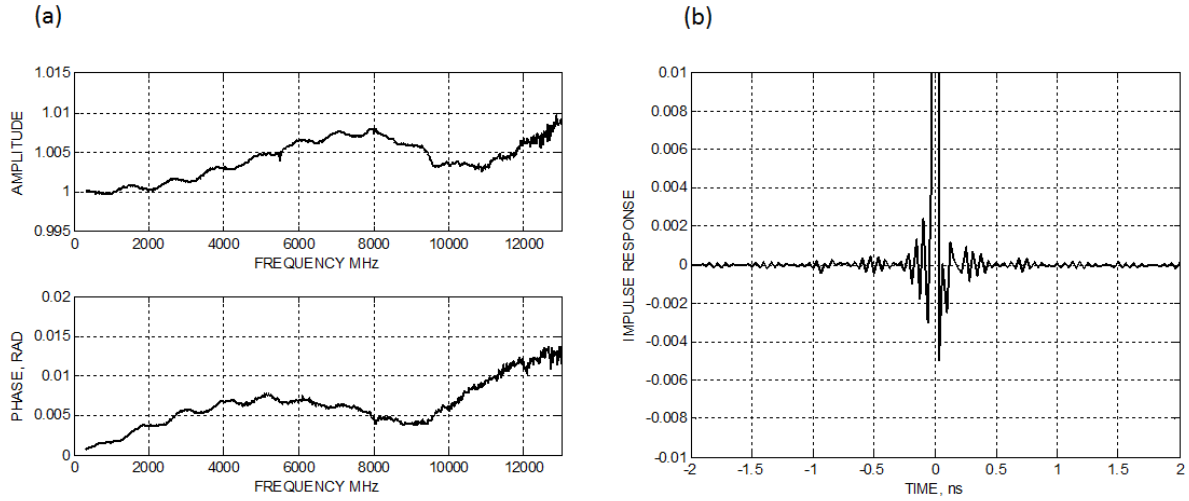

Figure 2 Inter-slice frequency response (a) and impulse response (b) for 32 GS/s composite ADC.

When all slice distortions are compensated, samples of each sub-ADC are combined in adders, resulting in Pre-I and Pre-Q samples. Overall ADC frequency response resulting from sub-ADC mismatch compensation is corrected by "common equalizer". In our simulations common equalizer with 115 FIR taps achieves 0.1% EVM using decimation factor of 10.

Figure 3 shows simulation of QAM-64 EVM for 32 GS/s composite ADC having 2 sub-ADCs, one 7-tap misalignment equalizer and 115 tap common equalizer. The QAM-64 signal with 2 GHz bandwidth was down-converted with a decimation factor of 10 and swept within the bandwidth of the ADP7000 digitizer. Since slice misalignment is relatively small, EVM degradation without slice correction is only 0.5% and occurs around 8 GHz region (spurious reflection from 16 GHz frequency). However, using only 7-tap misalignment FIR achieves 0.12% EVM baseline, eliminating slice distortions.

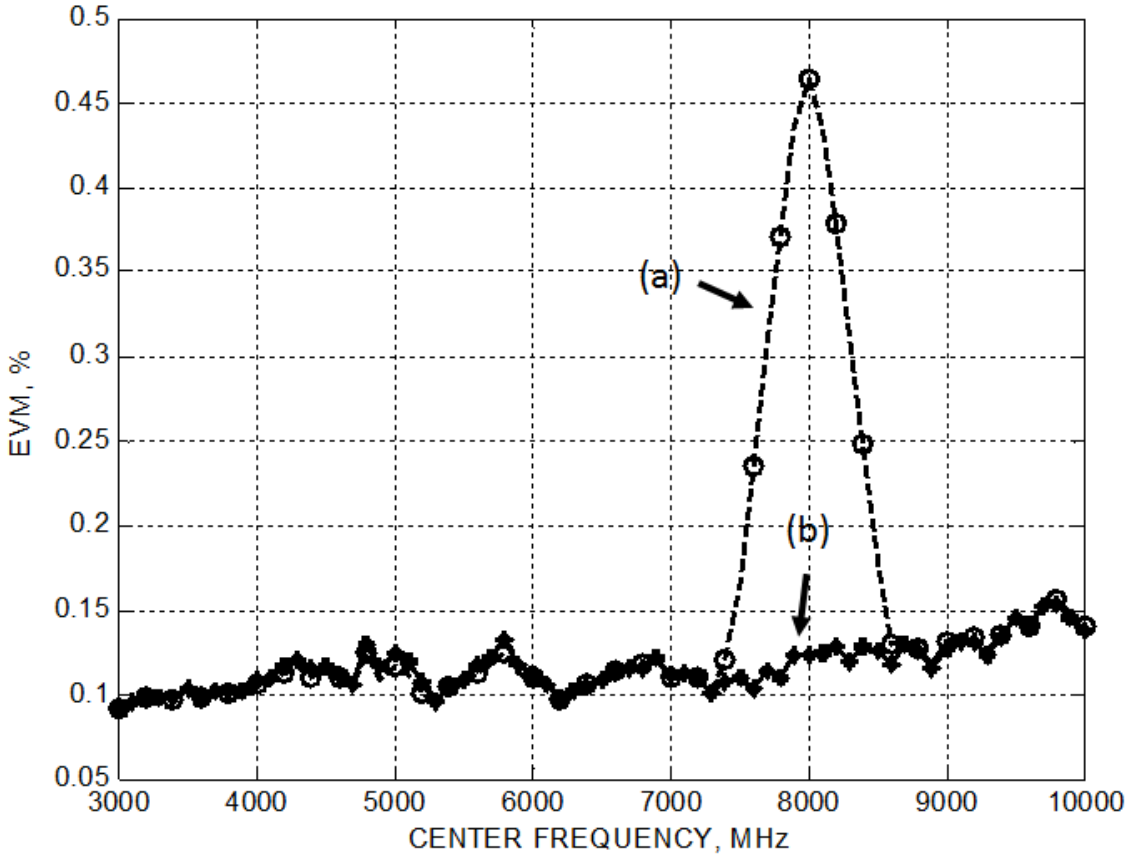

Fig. 3 QAM-64 EVM simulation for 32 GS/s composite ADC with 2 sub-ADCs; (a) – without misalignment correction; (b) – with 7 taps misalignment correction.

Similar results were obtained for 4 ADC slices running at 32 GS/s (Figure 4). Uncorrected EVM shows two major spurious reflections: from 16 GHz and 8 GHz, degrading EVM around 8 and 4 GHz. Using 3 misalignment equalizers with 7 taps followed by 115 taps common equalizer achieves 0.1% EVM baseline, resulting in nearly ideal EVM reconstruction, limited only by accuracy of square root cosine filter.

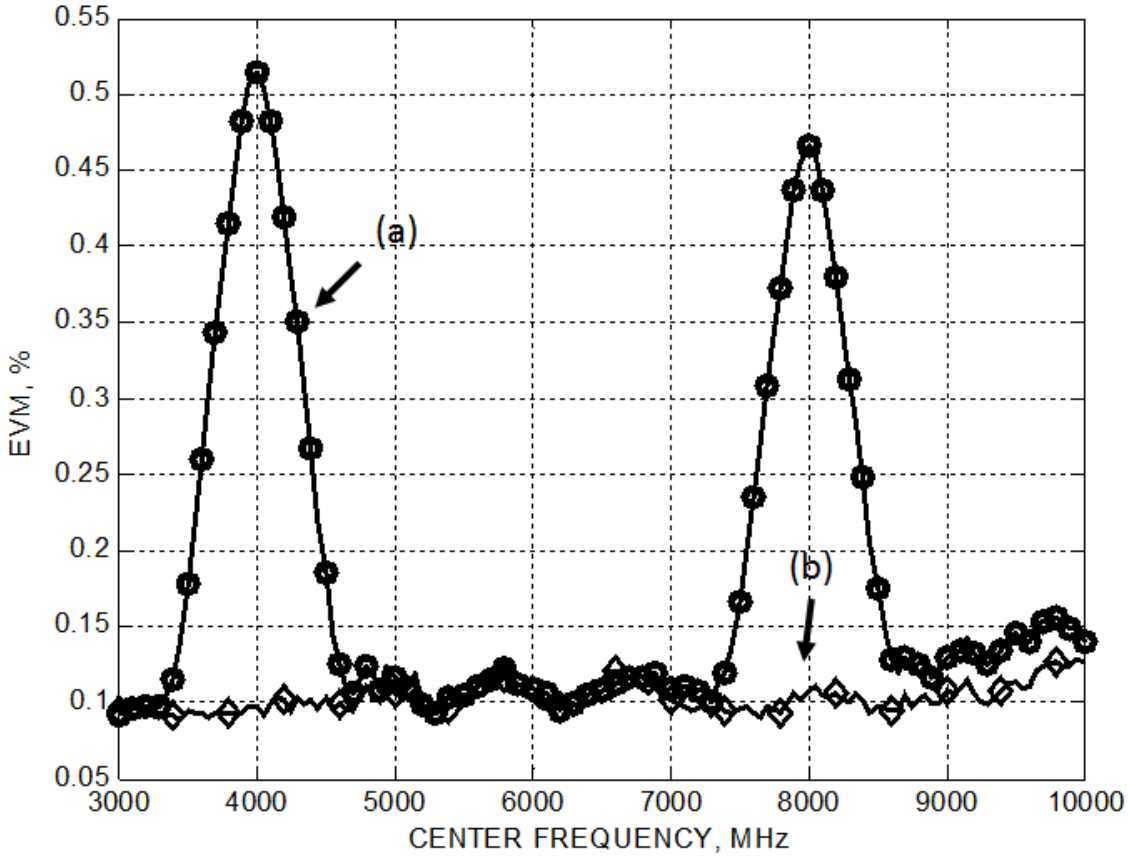

Fig.4. QAM-64 EVM simulation for 32 GS/s composite ADC with 4 sub-ADCs; (a) – without misalignment correction; (b) – with 3 misalignment equalizers using 7 taps.

References

[1]. "Real-time Digital Down-Conversion with equalization"

https://www.guzik.com/documents/products/Guzik_Real-Time_Digital_Down_Conversion_with%20Equalization.pdf

[2] A. Stein, L. Viitas, "Digital Equalization of mmWave Analog Frequency Up and Down-converters", Microwave Journal, April 2018). http://www.microwavejournal.com/articles/30099-digital-equalization-of-mmwave-analog-frequency-up-and-down-converters

[3] A. Stein, S. Volfbeyn, A.Taratorin. U.S. Patent 10,305,707 B1 "Digital Down Converter with Baseband equalization", Guzik Technical Enterprises, May 2019.