

# Real-Time Digital Down-Conversion with Equalization

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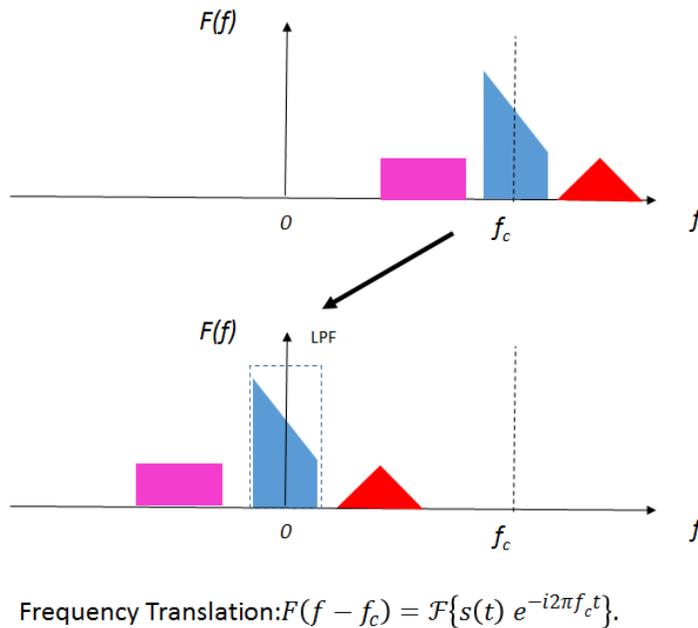
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## DOWN CONVERSION PRINCIPLE

Down conversion is basic operation in communications and signal processing. Down-converters perform a transformation of radio frequency (RF) signal into a baseband signal centered at the zero frequency. Digital down converters are used in high performance equipment, providing ultimate quality: ideal mixer without non-linear distortions, phase noise or temperature stability problems, fully controllable filters and decimation, possibility of programmable digital channel equalization. However, digital down conversion requires high speed analog-to-digital converter (ADC) and real time data processing.

The principle of down-conversion is based on frequency shift property. If arbitrary signal  $s(t)$  is multiplied by complex exponential  $e^{-i2\pi f_c t} = \cos(2\pi f_c t) - i \cdot \sin(2\pi f_c t)$ , then the frequency spectrum of this product is shifted down by  $f_c$ . Mathematically this “frequency shift” property is defined via Fourier Transform (signal spectrum): For  $F(f) = \mathcal{F}\{s(t)\}$  we get  $F(f - f_c) = \mathcal{F}\{s(t) e^{-i2\pi f_c t}\}$ .

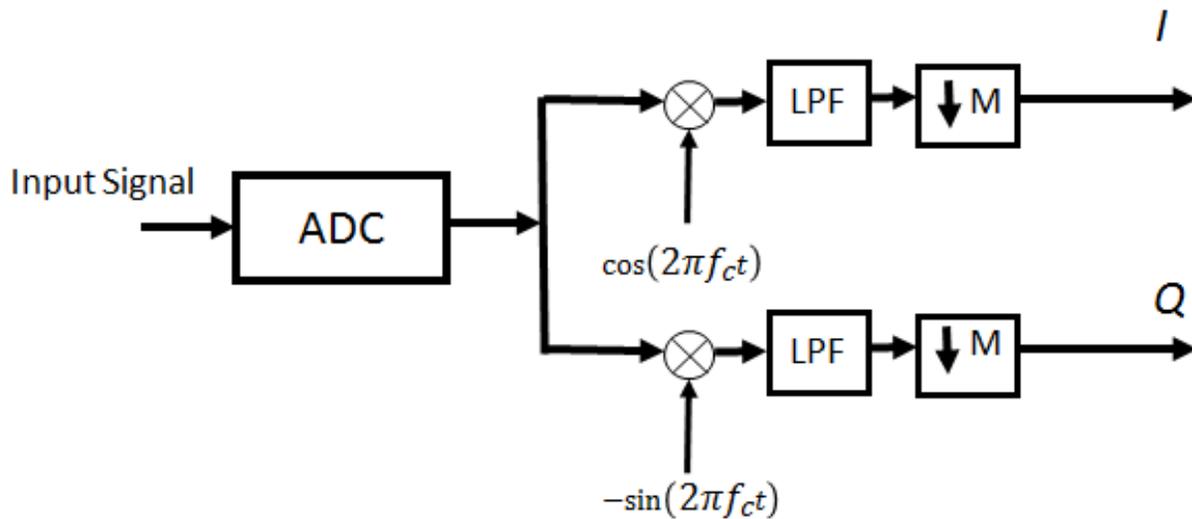
Spectrum shift during down-conversion is schematically illustrated in Fig.1, where signal is centered at center frequency  $f_c$  and occupies RF band, shown by blue. After down-conversion this spectrum becomes centered at zero frequency.



**Figure 1. Down-conversion: spectrum frequency shift and rejection of unwanted signals using low pass filtering.**

Since interference signals may be present in the spectrum (shown by red and magenta shapes), they need to be rejected after frequency translation. This is done by low-pass filtering which selects bandwidth of interest. Low pass filtering also allows reduction of sampling rate (decimation). Down-converted signal occupies relatively narrow frequency band and can be resampled at lower sampling rate without loss of information (sampling rate is determined by Nyquist theorem). After this procedure we get in-phase (I) and quadrature (Q) signal samples, corresponding to cosine and sine terms. These I/Q pairs retain all information of the original RF spectrum and can be used for signal demodulation.

Standard digital down-conversion block diagram is shown in Fig. 2 and consists of high-speed ADC, digital IQ mixer, performing signal multiplication on sine and cosine signals, low pass filters and decimators by factor of M. These operations can be implemented in real time using present-day FPGAs.



**Fig.2 Standard digital down-conversion block diagram.**

## THE NEED FOR EQUALIZATION

Even though the digital down-conversion operations (digital mixer, low pass filtering/decimation) are mathematically ideal, it does not necessarily mean that we will automatically get high quality demodulated I/Q signals. High sampling rate ADC will inevitably have non-uniformity of frequency response which causes significant degradation of demodulated signal quality.

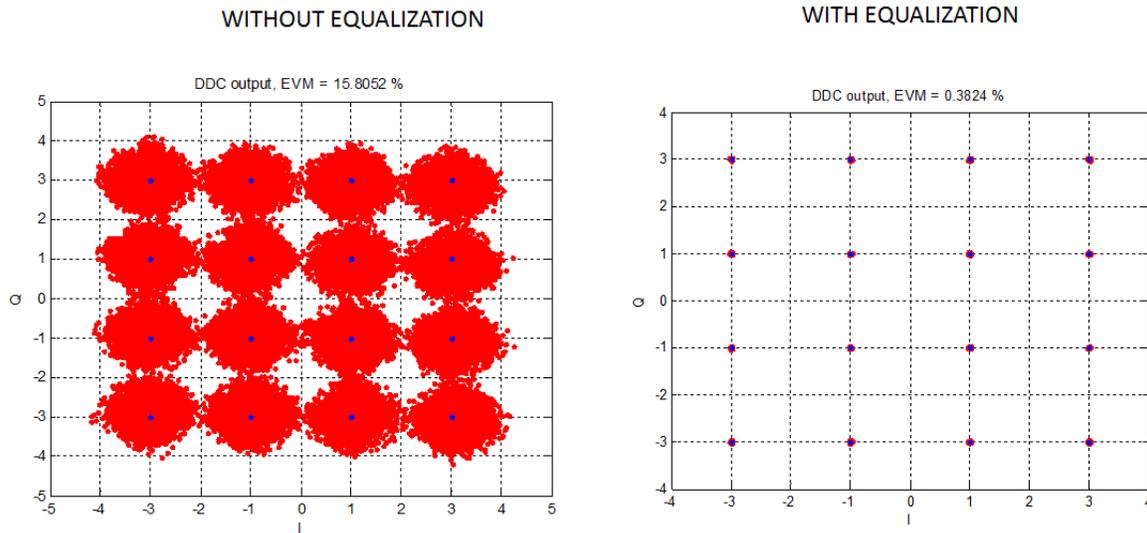
Quality of down-converted signal can be estimated using modulation, for example quadrature amplitude modulation (QAM). I/Q samples of QAM signal have discrete amplitude values. For example, QAM16 modulation has 4 discrete values for in-phase and quadrature samples, resulting in 16 values on I/Q plane (constellation diagram). The constellation diagram for QAM16 (quadrature amplitude modulation with 16 levels) is shown in Figure 3(b), for 1 GHz-wide down

conversion. This constellation diagram is obtained using simulated QAM signal, distorted by measured ADC frequency response with subsequent digital equalization.

Demodulation quality is usually measured using EVM (error vector magnitude). For each pair of demodulated samples  $[I_k, Q_k]$ , with corresponding ideal values  $[I_{k_0}, Q_{k_0}]$ , the magnitude (length) of error vector equals  $E_k = \sqrt{(I_k - I_{k_0})^2 + (Q_k - Q_{k_0})^2}$ . The reference vector length  $V_k = \sqrt{I_{k_0}^2 + Q_{k_0}^2}$ . The percentage of EVM is defined by the following summation:

$$EVM\% = \sqrt{\frac{\sum_k E_k^2}{\sum_k V_{kref}^2}} * 100$$

EVM for Figure 3(b), is low and equals 0.38%. When equalizing filter is disabled, demodulated signal is shown in Fig. 3(a) with unacceptably high EVM of almost 16%.



**Figure 3. QAM 16 constellation diagrams. Without equalization EVM is 15.9%, with equalization EVM=0.38%**

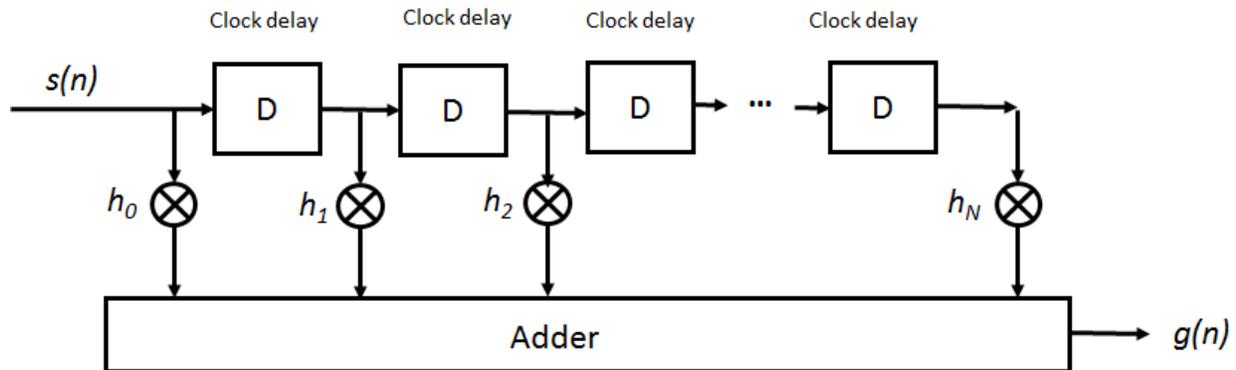
High speed digitizers need to be equalized to pre-determined reference frequency response. In this case results of sampling and demodulation are consistent and digitizer can be used as reference measurement device.

The principle of digital equalization is based on constructing digital filter with frequency response, compensating frequency response of measurement system. Equalizer is usually implemented as Finite Impulse Response (FIR) filter.

FIR filter forms filter output  $g(n)$  as weighted sum of input ADC samples  $s(n)$

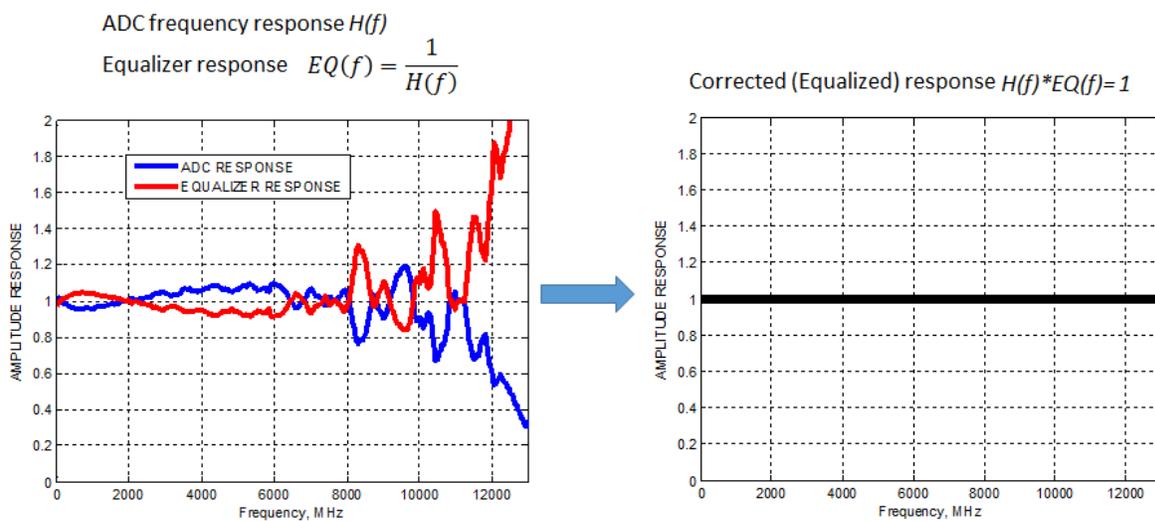
$$g(n) = \sum_{m=0}^N h_m s(n - m)$$

FIR filter operating on ADC samples and having  $N+1$  taps is implemented by  $N+1$  multipliers with weights  $\{h_0, h_1, \dots, h_N\}$  (Filter impulse response coefficients) and adder.



**Figure 4. Implementation of FIR filter using delays, multipliers and adder**

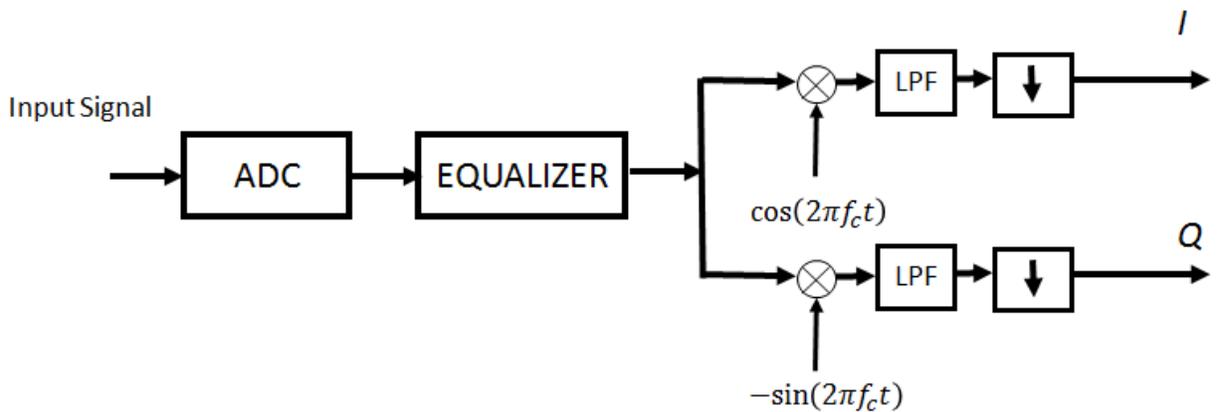
The equalization principle is shown in Fig. 5. Equalizer taps are calculated so that frequency response of equalization filter response  $EQ(f)$  is inverse of channel frequency response  $H(f)$  i.e.  $EQ(f) = \frac{1}{H(f)}$ . After filtering operation amplitude and phase distortions are compensated, resulting in flat amplitude frequency response and linear phase.



**Figure 5. Principle of equalization – compensating frequency response using inverse filtering**

Equalization may be performed at ADC sampling rate (high frequency equalizer) before down-conversion, or after down conversion.

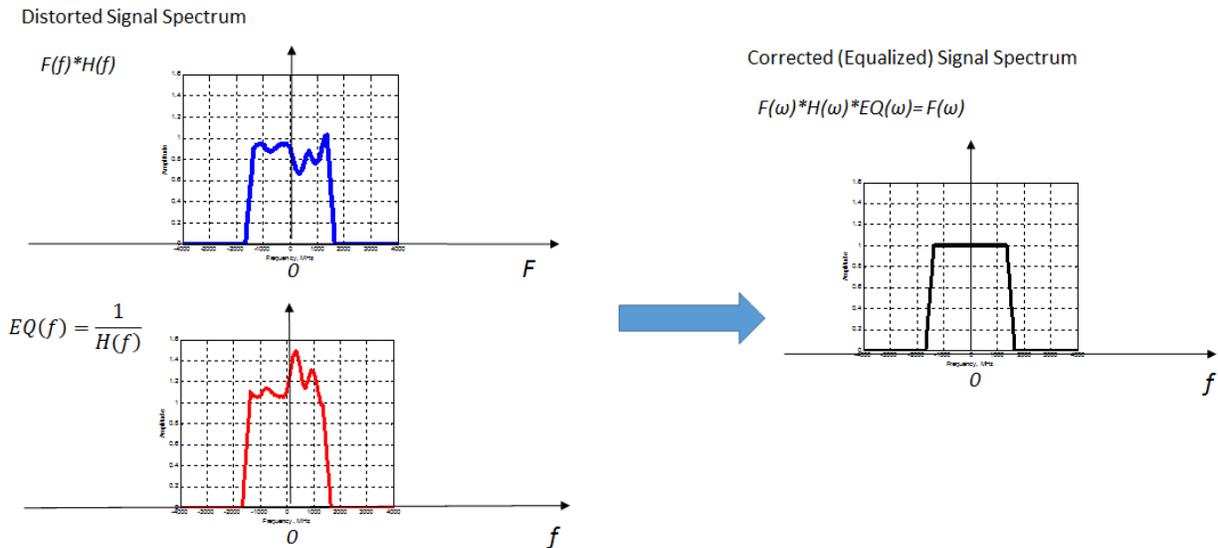
Figure 6 shows digital down-conversion system with high frequency equalizer.



**Figure 6. Equalization filter at ADC sampling rate (before down-conversion)**

In this configuration all frequencies in the ADC bandwidth are corrected, however filtering operation need to be performed at high ADC sampling rate. For example, at ADC operating at 40 GSa/s a 160 taps-long equalizer requires 160 multiplications for each incoming ADC sample (25 ps). The most resource-consuming components of FIR filter are multipliers. Frequency of operation of present-day circuits (e.g. FPGAs) is up to 200-500 MHz. This frequency is much lower than ADC sampling rate, therefore, each multiplication in the FIR filter is carried out by a group of multipliers connected in parallel. The required number of multipliers becomes the main reason that makes it necessary to use more processing resources, or, in some cases, makes the real time equalizer design impossible.

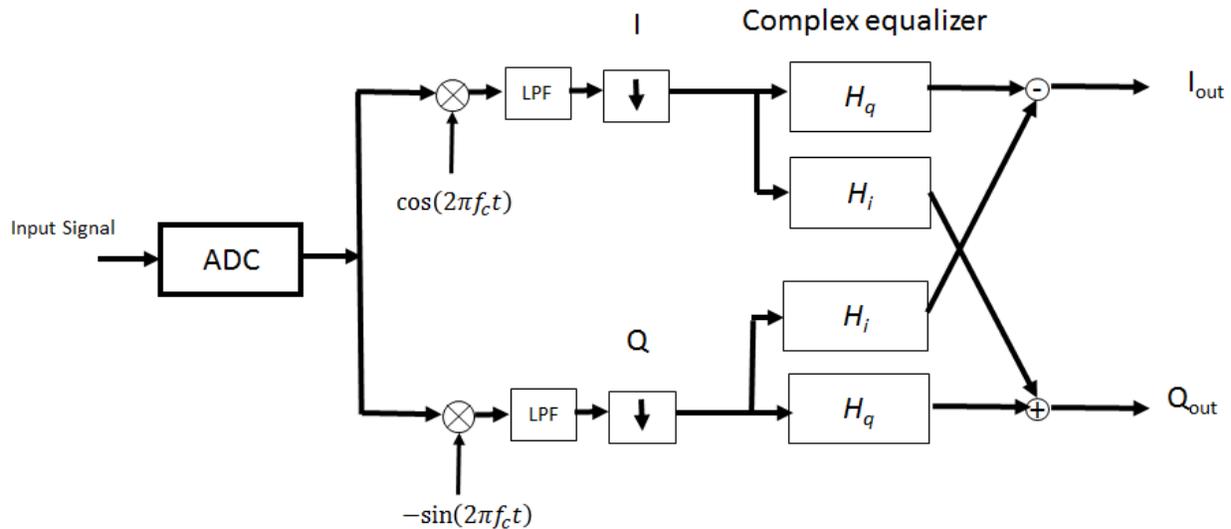
Since signal of interest occupies only narrow frequency range, equalization may be performed after digital down conversion (performing frequency response correction only in a range of frequencies centered at zero), as shown in Figure 7.



**Figure 7. Equalization filter compensates distortions in narrow band centered at zero frequency (after down-conversion)**

Note that spectrum shown in Fig.7 has “negative” frequencies, since down-converted signal is complex, represented by quadrature I/Q pairs of samples. This means that filtering need to be applied to real and imaginary signals, and equalizing filter also becomes complex, having real  $Hq$  and imaginary  $Hi$  parts. This equalizer is directly implemented as four real-valued FIR filters.

The block diagram of down-conversion with equalizer is shown in Figure 8. This implementation has several major advantages. The filtering operation is performed at low sampling rate (after decimation) and becomes feasible for real-time implementation. Smaller FIR length (and smaller number of multipliers) can be used without compromising signal quality. This is due to the fact that after decimation by  $M$  (i.e. retaining only  $M$ -th signal samples), filter impulse response is also reduced by a factor of  $M$ . For example, for decimation ratio  $M=20$ , 200 taps-long FIR at full ADC sampling rate becomes equivalent to FIR with  $200/20=10$  taps. However four FIR filters are required. Number of filters may be reduced to 3 using linear combination of I/Q samples.

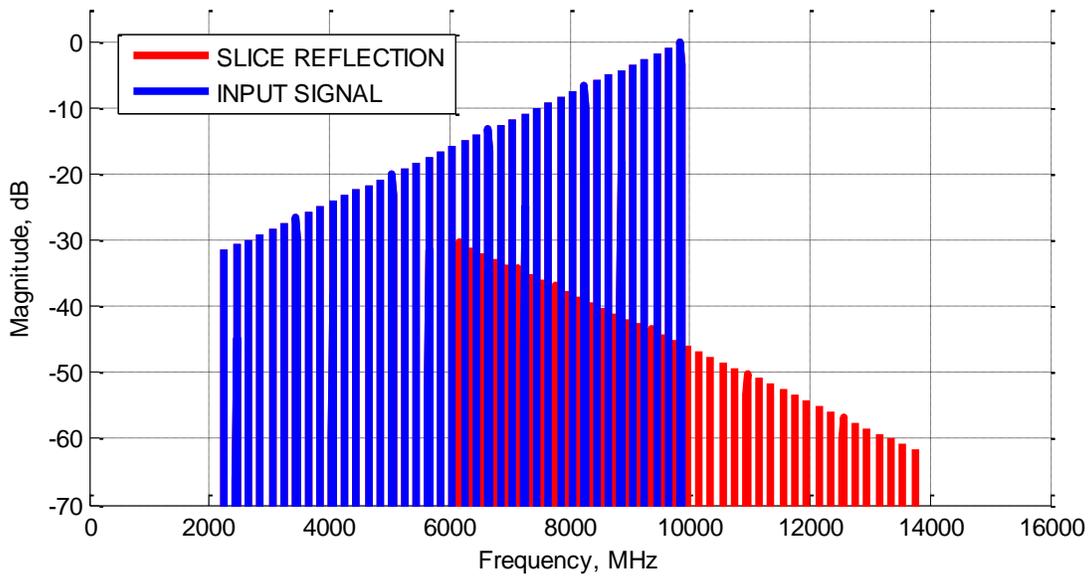


**Figure 8. Digital down-conversion with equalization of down-converted signal. Four-branch FIR equalizer is required to process I and Q samples**

## SLICE (INTERLEAVED) ANALOG TO DIGITAL CONVERTERS

Most of high speed analog to digital converters are built as composite ADC's that consist of a number of time-interleaved sub-ADC's (slices) with a common input and sequential timing. The amplitude and phase frequency responses of these sub-ADC are not identical, resulting in signal distortions, such as appearance of multiple spurious frequency components. Some of these spurious components may cause significant degradation of demodulated signal quality.

Based on interleaved ADC theory, signal spectrum at ADC output consists of sum of frequency responses for all individual slices with complicated frequency and phase shift terms. An example shown in Figure 9 demonstrates error signal for multi-tone input signal (blue) covering 2-10 GHz range for 32 GSa/s ADC structure consisting of two slices. Mismatch of ADC slice frequency response causes erroneous spectrum components (red), reflected from 16 GHz (1/2 sampling rate). For multi-slice ADCs resulting spectrum superposition becomes complicated, generating multiple spurious components and causing signal degradation.



**Figure 9. Example of spurious components for 2-slice 32 GSa/s ADC(a). Slice frequency response mismatch causes spectrum reflection from 16 GHz (red).**

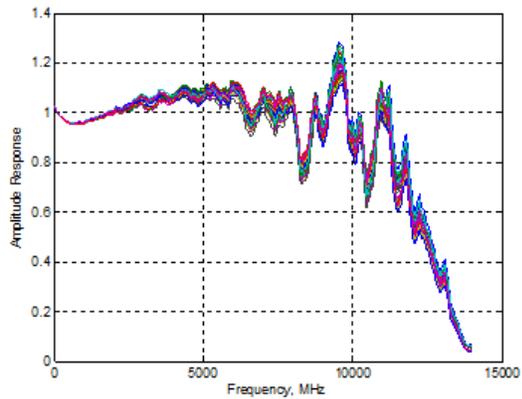
#### SUB-ADC FREQUENCY RESPONSES AND CORRECTION OF ADC SLICE DISTORTIONS

Each individual sub-ADC frequency response is measured during ADC calibration. Amplitude response is obtained by sweeping sine wave using signal generator. Group delay measurement is based on method described in [1] and [2], and allows accurate high resolution measurement of group delay and phase response

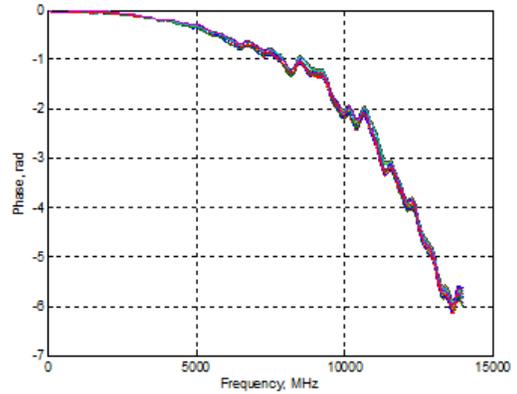
Figure 10 shows superposition of amplitude and phase responses of 40 individual sub-ADC slices measured using Guzik 40 GSa/s ADC6000 8-bit digitizer in the range up to 15 GHz (top graphs). Bottom graphs show ratio of individual slice amplitude responses to average frequency response (left) and difference of individual slice phase response relative to average (right). As seen, frequency response deviations become considerable above 5 GHz, with amplitude deviations more than 10% and phase deviations exceeding 0.1 radian.

Depending on slice amplitude and phase responses misalignment, this ADC slice structure may cause significant degradation of down-converted signal. Figure 11 shows EVM calculation (simulation) for 1 GHz RF band down-converted from 10 GHz carrier using FIR equalizing filter with 321 taps (based on ADC6000 frequency response shown in Figure 10).

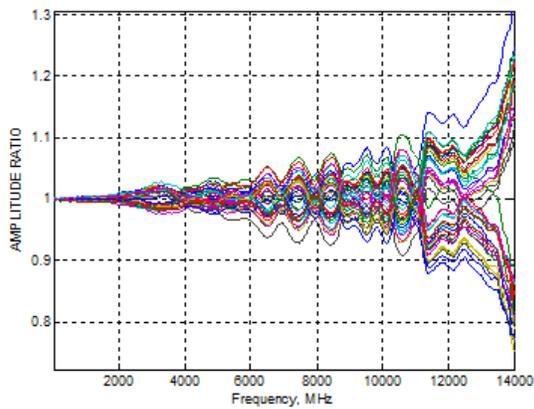
Amplitude Response, 40 ADC slices



Phase Response, 40 ADC slices



Deviation of Amplitude Response



Deviation of Phase Response

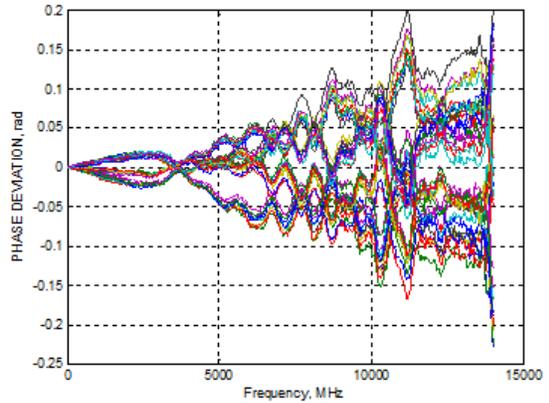
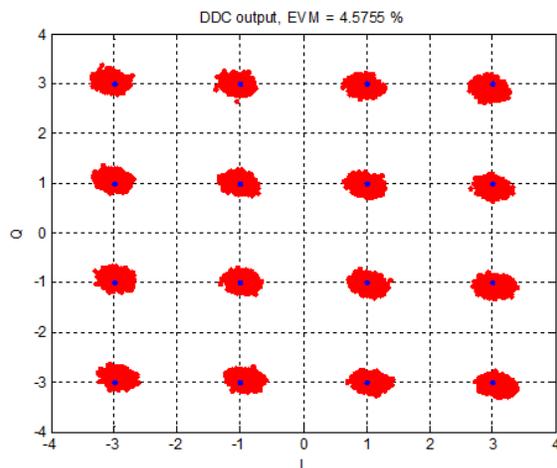
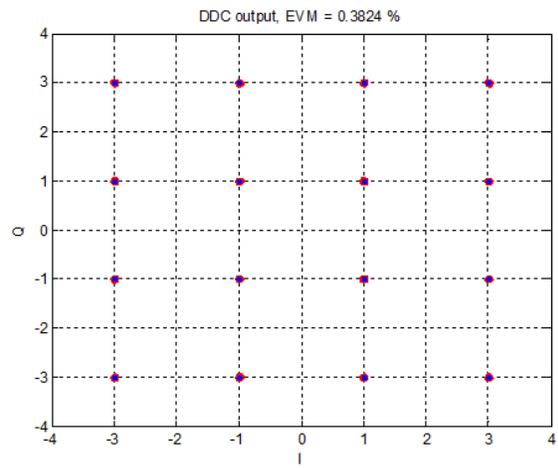


Figure 10. Amplitude and phase responses and deviations for 40 sub-ADC slices (ADC6000 Digitizer)

SLICE EQUALIZATION DISABLED



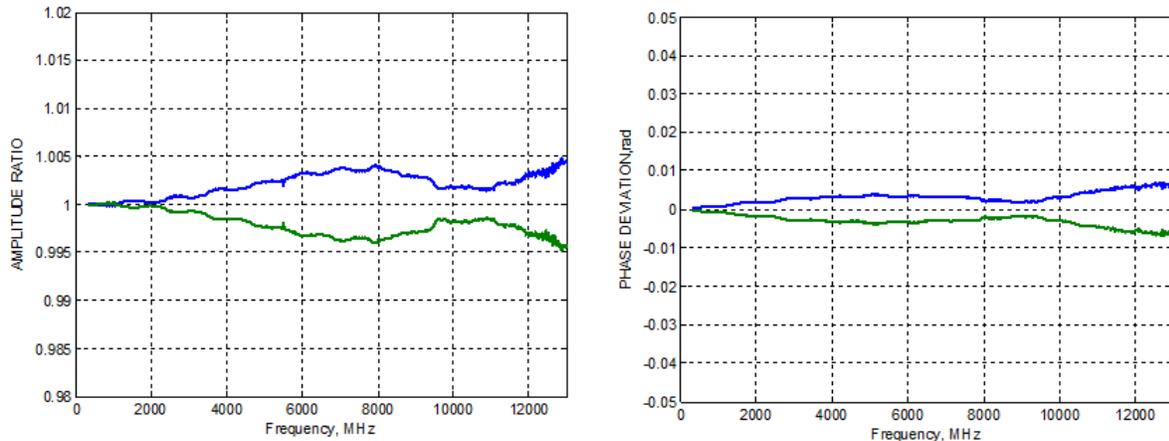
SLICE EQUALIZATION ENABLED



### Figure 11. Impact of sub-ADC slice distortions on EVM

When slices are ignored and ADC frequency response is approximated by average amplitude and phase, EVM exceeds 4.5%. When per-slice equalization is enabled, EVM is reduced to 0.38%.

Newer 32 GSa/s Guzik ADP7000 series 10-bit digitizer allows improved calibration and alignment of sub-ADC frequency responses. After proper calibration procedure, the ADP7000 digitizer is represented by two 16 GSa/s slices, corresponding to ADC chip quadrants. Amplitude and phase responses within each quadrant are aligned with high accuracy during ADC calibration procedure. Figure 12 shows deviations of amplitude and phase responses between quadrants measured during ADC calibration. As seen, amplitude and phase deviations are smaller compared to ADC6000 series digitizer, with amplitude deviation less than 0.5% and maximum phase deviation below 0.01 rad. However, even these small amplitude and phase misalignments result in considerable EVM degradation (for example, 1.2% without slice correction, 0.3% with slice correction enabled).



**Figure 12. Amplitude and Phase response slice deviation for ADP7000 digitizer**

Fundamental limitation of ADC slice structure is that slice distortions cannot be compensated by a linear equalizing filter. Therefore, they set hard limit to achievable demodulation quality and must be corrected during ADC equalization procedure.

Correction of ADC slice distortions is disclosed in [3] and was described in Guzik Technical Enterprises white paper [4]. This paper also illustrates inevitable generation of spurious spectrum components caused by ADC slice misalignment. ADC slice equalization is achieved by using time-varying equalizing filter operating at full ADC sampling speed. Each incoming ADC sample corresponding to ADC slice  $n$  is convolved with pre-calculated  $n$ -th FIR filter. Total number of pre-calculated FIR filters is equal to the number of ADC slices and FIR filter coefficients are changed for each ADC sample. Block-diagram of down converter with slice equalization is similar to Figure 6, however equalizer becomes time-variant system, changing for each ADC sampling clock. This method achieves suppression of spurious components, however it requires FIR filtering

at full ADC speed and cannot be combined with down-conversion due to the limited amount of FPGA resources.

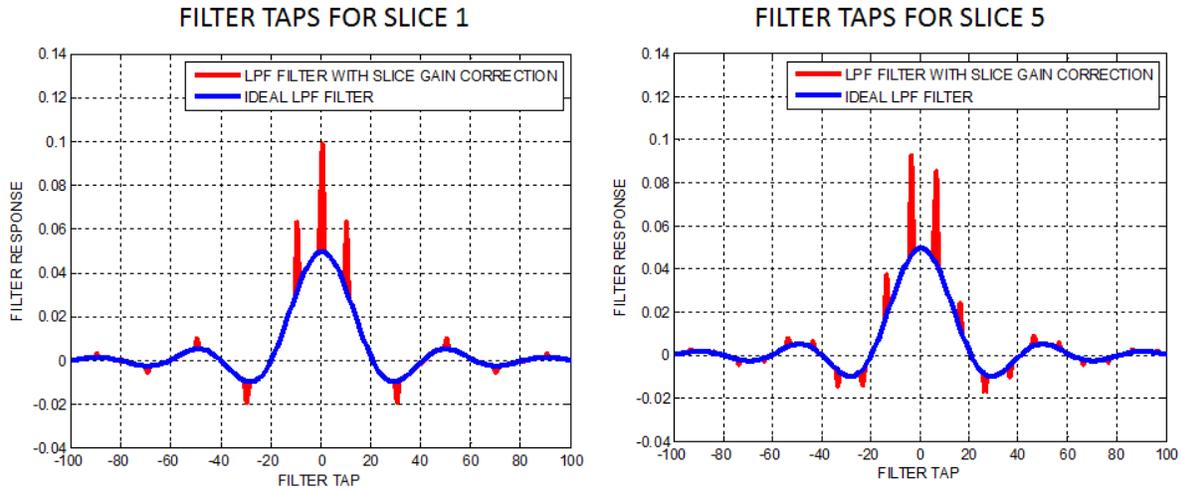
It would be highly advantageous to apply slice correction to decimated down-converted samples, however direct solution of this problem is not possible. The problem is that low pass filtering propagates high frequency slice distortions to multiple down-converted samples by combining and averaging samples coming from different ADC slices. Distortions, generated by sub-ADCs become not correctable because inter-slice distortion information is lost. Therefore, in order to equalize slice distortions we need to find a way of processing original high sampling rate stream of ADC samples.

## REAL-TIME DIGITAL DOWN-CONVERSION WITH SLICE EQUALIZATION

A general method for achieving interleaved ADC correction at reduced data rate was disclosed in [5,6] This method is based on implementing time-varying FIR equalization filter, operating on ADC samples acquired at full ADC sampling clock. However, FIR filtering operation is performed at low sampling rate in such a way, that each output of FIR filter corresponds to the corrected decimated sample. As a result, the equalization FIR operation can be performed at reduced clock rate, corresponding to decimation factor (e.g. at 1.6 GSa/s instead of 32 GSa/s for decimation factor 20). This allows real-time implementation using available resources.

A simplified illustration of this method will be given below for idealized model. Assume that ADC consists of 40 slices, having unity slice frequency responses and gains (ideal flat frequency response), except for slices 1, 11, 21 and 31 having gains 0.5. It is obvious, that “slice correction” in this case can be achieved simply by multiplying each 10-th ADC sample by 2.

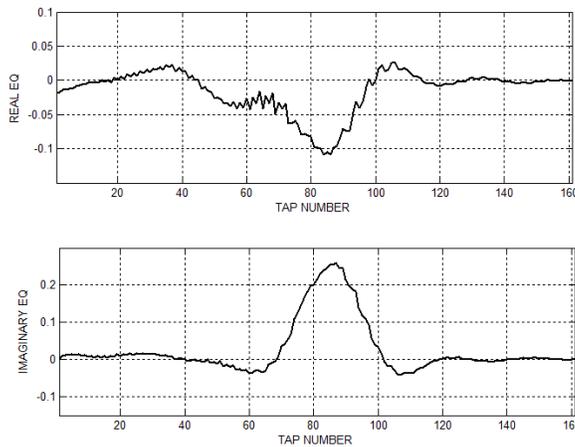
Consider down-conversion block diagram shown in Figure 2. We can incorporate samples gain correction into low pass filter coefficients. For example, for samples coming from ADC slice 1 (i.e. samples 1, 41, 81 etc) we need to apply standard coefficients of low pass filter (blue graphs on Figure 11) and multiply each 10-th coefficient by 2. In this case center filter tap has double amplitude, as well as symmetrical taps for samples shifted by 10 ADC samples. Similarly, for sample, coming from ADC slice 5 double amplitude taps will become shifted by 4 samples relative to slice 1. The result is shown by red curve on Figure 13.



**Figure 13. Low pass filter coefficients for ADC with slice gain mismatch**

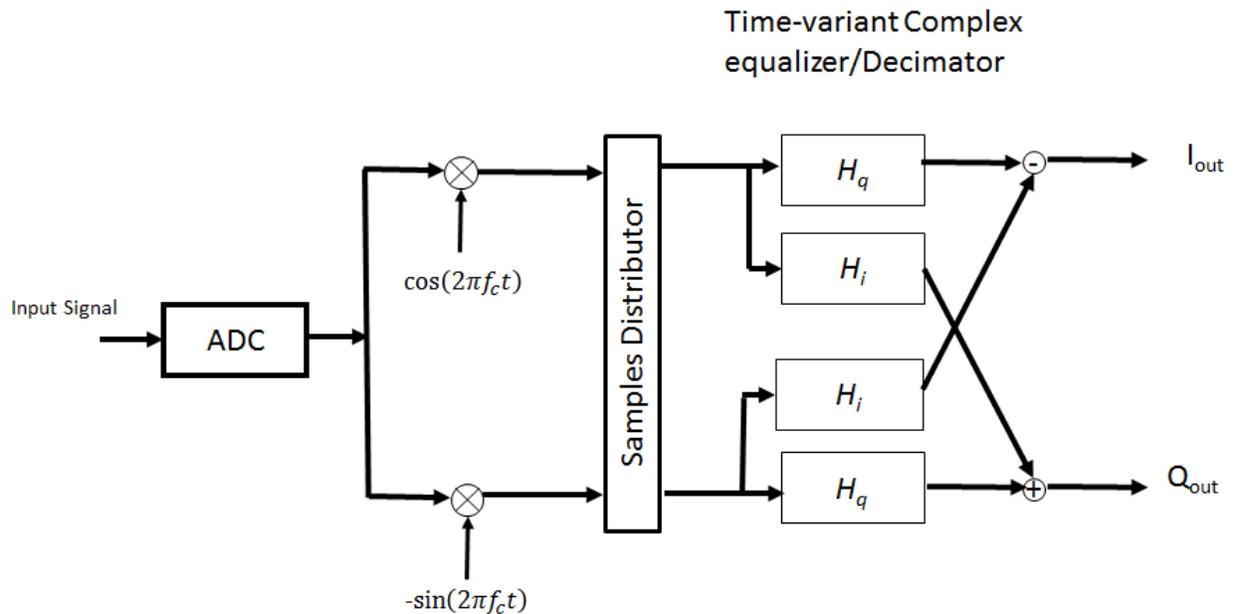
While FIR filter processes original stream of high speed ADC samples, the full FIR calculation result is required only for decimated samples. For example, if we use decimation ratio 10, FIR combining low-pass anti-aliasing filtering and slice gain correction is applied to samples corresponding to slices 1, 11, 21 etc. Calculations for samples 2-10,12-20 etc are not performed. Thus, we can decrease processing speed by a factor of 10.

The method for calculating equalizer response, including amplitude and phase responses of each sub-ADC slices is described in [5]. The calculated FIR taps incorporate correction of amplitude and phase distortions introduced by adjacent slices. At the same time, FIR output provides anti-aliasing filtering. This can be visualized by experimental sets of 161 taps used for down conversion of 10 GHz center frequency with decimation factor 20. Figure 14 shows real and imaginary equalizer coefficients (161 taps) calculated for given amplitude and phase slice responses. Small zig-zag features in real and imaginary equalizer coefficients correspond to amplitude and phase distortions introduced to a particular ADC sample by adjacent sub-ADC samples.



**Fig.14 Real and imaginary FIR equalizer taps for ADC slice 1 (down conversion from 10 GHz)**

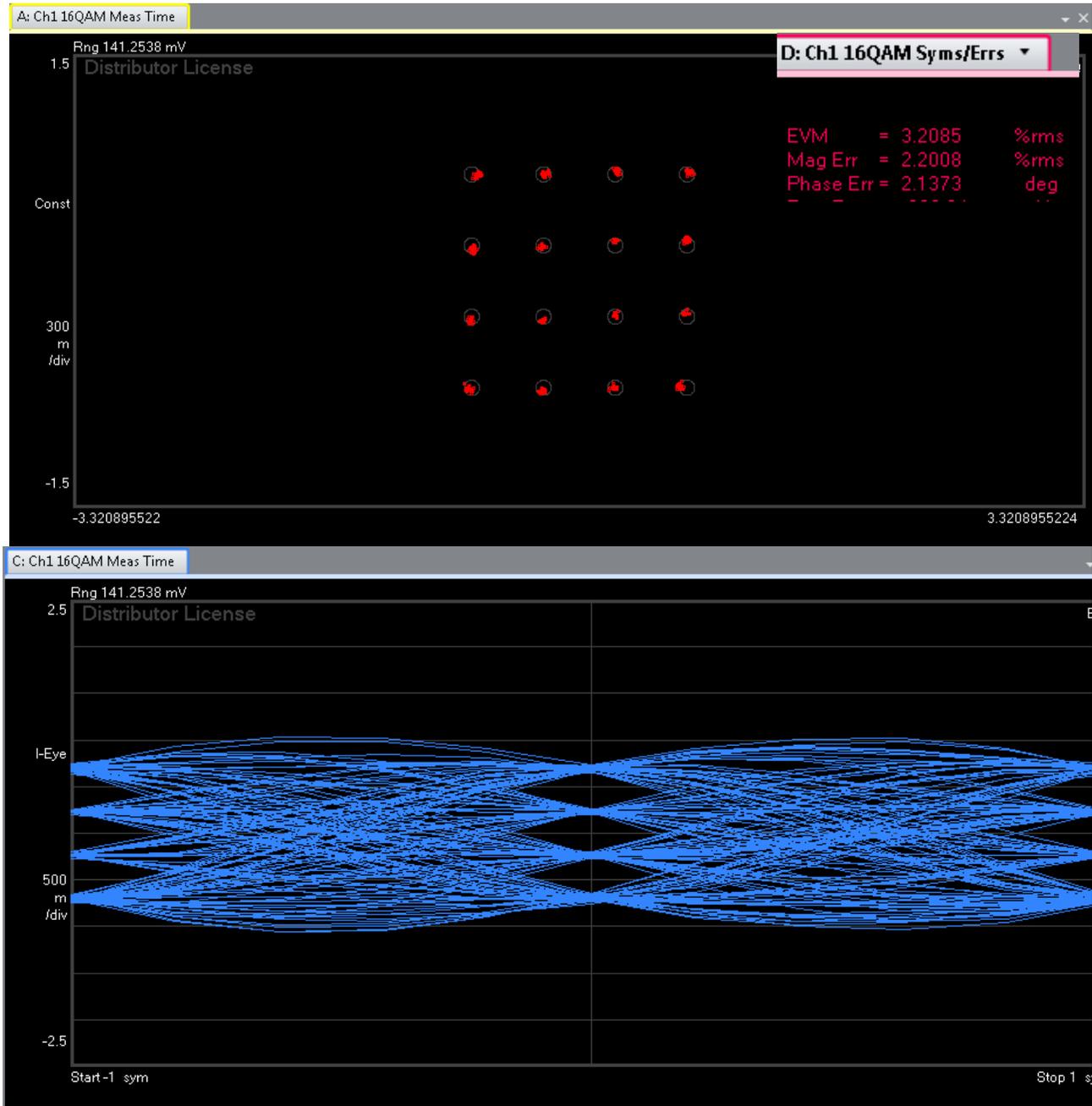
A simplified block-diagram of real-time down-conversion with slice correction and equalization is shown in Figure 15.



**Figure 15. Block diagram of real-time down-converter with slice equalization**

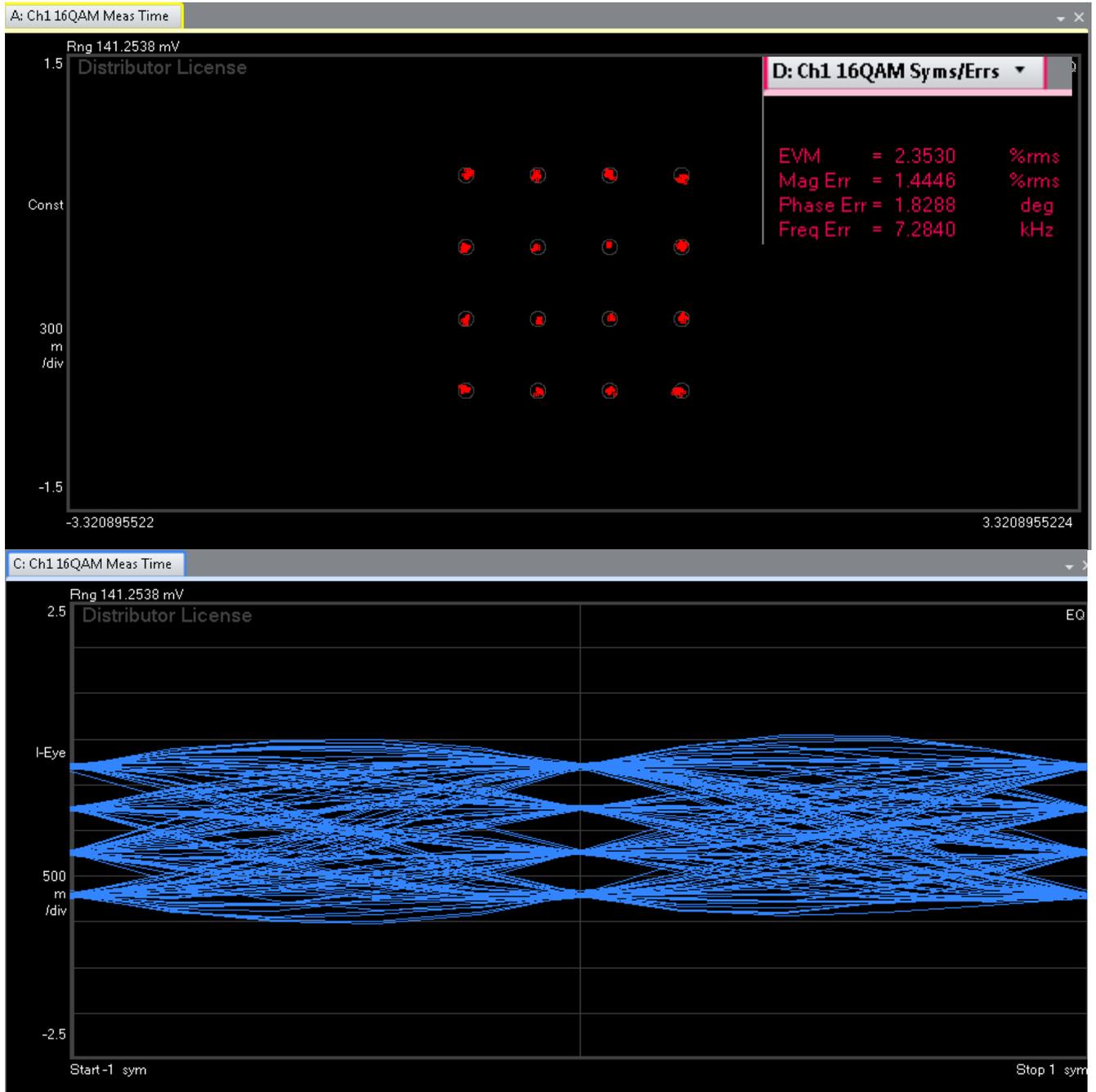
The system shown in Fig.15 consists of high-speed ADC, mixers and samples distributor system, which supplies correct sequence of samples to time-variant complex equalizer. Equalizer combines slice corrected frequency response equalization, low-pass anti-aliasing filtering and decimation. Coefficients of complex equalizer change depending on the ADC slice number corresponding to decimated output value.

This method is implemented in the ADP7000 series digitizers as “Advance Real-time DDC” option `ADC_ADDCRT1`, operating at 32 GSa/s. Examples of real-time down conversion are shown below.



**Figure 16. ART-DDC Real-time Down Conversion, QAM16, 8 GHz carrier, 1.76 GSymbols/s data rate; Slice Equalization disabled, EVM=3.2%**

Figure 16 shows screen capture from VSA software – result of real-time down-conversion using ADP700 32 GSa/s digitizer with slice equalization disabled. Frequency response of the equalizer in this case corresponds to average of two sub-ADC slices, with de-embedded frequency response of cables/connectors. Symbol rate 1.76 GSa/s, carrier frequency equals 8 GHz. RF Signal was generated using arbitrary waveform generator operating at 64 GSa/s data rate. Residual EVM equals 3.2 %.



**Figure 17. ART-DDC Real-time Down Conversion, QAM16, 8 GHz carrier, 1.76 GSymbols/s data rate; Slice Equalization enabled, EVM=2.35%**

Figure 17 shows down-conversion results with ADC slice equalization enabled. Residual EVM is reduced to 2.35%. This lowest achievable EVM is mainly limited by performance of the arbitrary waveform generator used as the modulated signal source.

To summarize, ADC slice structure may cause significant EVM degradation, which is not correctable using additional (e.g. adaptive) equalization. Therefore, real-time digital down-conversion with ADC slice equalization is essential for achieving high down-converted signal quality.

## References

- [1] U.S. Patent 9933467 “Group delay measurement apparatus and method”, 2018, Guzik Technical Enterprises
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- [3] U.S. Patent 7,408,495 “Digital Equalization of multiple Interleaved analog-to-digital converters”, 2006, Guzik Technical Enterprises
- [4] S. Volfbeyn, A. Stein “ Equalization of Multiple Interleaved Analog-to-Digital Converters (ADC’s) [https://www.guzik.com/documents/products/guzik\\_equalization\\_of\\_multi\\_adcs\\_1.pdf](https://www.guzik.com/documents/products/guzik_equalization_of_multi_adcs_1.pdf)
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