

Equalization of Multiple Interleaved Analog-to-Digital Converters (ADC's)

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1 Introduction

Multiple interleaved Analog-to-Digital Converters (ADC's) are widely used to increase the sampling rate during the conversion process. In order to improve the interleaving, the DC offset, gain and clock timing are adjusted. However, these adjustments are not sufficient to achieve the best quality interleaving, especially in the high frequency range of the converted signals [1]. The reason is the difference in the amplitude frequency responses and in the group delay frequency responses of the individual ADCs. It is impractical to equalize the frequency responses of ADCs in the analog path of the front end. So, a digital equalizer should be used after the interleaved ADC. This allows equalization of frequency responses close to the Nyquist frequency.

Fig.1 presents simplified block diagram of frequency response equalization. The amplitude frequency response and relative group delay frequency response of each ADC are measured with a signal from a calibration signal generator. The measurements are performed for multiple frequencies in the frequency range of the acquired analog signal. Based on this measurement the coefficients of the time variant interleaved equalizer are calculated. The equalizer may be realized as an FIR filter. The equalization coefficients are changed for each sample from each particular ADC. Typically the equalizer is implemented in a FPGA.

2 The Misalignment Distortions

2.1 The Input Signal

An interleaved ADC consists of M individual ADCs with the numbers $0, 1, \dots, i, \dots, M-1$. The input signal comes to each of the individual ADCs through a correspondent analog front end AFE. Each AFE contains devices that precede the individual ADC (an amplifier etc.) and the input analog circuits of the ADC itself. An AFE with the number i may be described by the transfer function $H_i(k)$. The output signals of the individual ADCs are combined together in an aggregate output signal by an interleaver. While an individual ADC has a sampling frequency F_{s_ind} the interleaved ADC offers an aggregate sampling frequency F_s that is M times higher than F_{s_ind} . The sampling interval of the composite ADC equals $T = 1/F_s$.

The analog signal $s_a(t)$ that comes to the input of the interleaved ADC may be expanded into Fourier series at a time interval $N*T$ (N is an arbitrary integer):

$$s_a(t) = \sum_{k=-\infty}^{+\infty} C_k * \exp(j*2*\pi*k*F_s/N*t). \quad (1.1)$$

The series coefficients C_k satisfy the next equation:

$$C_k = \int_0^{N*T} s_a(t) * \exp(-j*2*\pi*k*F_s/N*t) dt. \quad (1.2)$$

There is, as a rule, an antialiasing filter before the ADC with the cutoff frequency less than $F_s/2$, so that the coefficients C_k differ from zero only in the range $-N/2 \leq k < N/2$. In that case the equation (1.1) becomes

$$s_a(t) = \sum_{k=-N/2}^{N/2-1} C_k * \exp(j*2*\pi*k*F_s/N*t). \quad (1.3)$$

After passing through the correspondent AFE to the input of the individual ADC with the number i the analog signal $s_a(t)$ changes into signal $s_{ai}(t)$ with Fourier coefficients $C_k*H_i(k)$.

2.2 The Output of an Individual ADC.

The sequence of samples $x_i[m]$ at the output of the individual ADC with the number i may be linked to the Fourier coefficients C_k of the input analog signal $s_a(t)$ in the next way:

$$\begin{aligned} x_i[m] &= s_{ai}((m*M + i)*T) = \sum_{k=-N/2}^{N/2-1} C_k * H_i(k) * \exp(j*2*\pi*k*F_s/N*(m*M + i)*T) = \\ &= \sum_{k=-N/2}^{N/2-1} C_k * H_i(k) * \exp(j*2*\pi*k*(m*M + i)/N). \end{aligned} \quad (2.1)$$

The DFT $X_i(k)$ of the sequence $x_i[m]$ may be found as

$$X_i(k) = \sum_{m=0}^{L-1} x_i[m] * \exp(-j*2*\pi*k*m/L),$$

where $L = N/M$ is the number of samples that appear at the individual ADC output during the time interval $N*T$. Substitution of (2.1) into the last expression gives:

$$\begin{aligned} X_i(k) &= \sum_{m=0}^{L-1} \sum_{l=-N/2}^{N/2-1} C_l * H_i(l) * \exp(j*2*\pi*l*(m*M + i)/N) * \exp(-j*2*\pi*k*m/L) = \\ &= \sum_{m=0}^{L-1} \sum_{l=-N/2}^{N/2-1} C_l * H_i(l) * \exp(j*2*\pi*l*i/N) * \exp(j*2*\pi*(l-k)*m/L) = \\ &= \sum_{l=-N/2}^{N/2} C_l * H_i(l) * \exp(j*2*\pi*l*i/N) * \sum_{m=0}^{L-1} \exp(j*2*\pi*(l-k)*m/L). \end{aligned} \quad (2.2)$$

It is well known that

$$\begin{aligned} \sum_{m=0}^{L-1} \exp(j*2*\pi*(l-k)*m/L) &= L, \text{ if } (l-k)\%L = 0, \text{ and} \\ \sum_{m=0}^{L-1} \exp(j*2*\pi*(l-k)*m/L) &= 0 \text{ otherwise.} \end{aligned} \quad (2.3)$$

Therefore the non zero terms in the equation (2.2) have an index $l = k + p*L$, $-N/2 \leq p < N/2$, so that

$$X_i(k) = L * \sum_{p=-M/2}^{M/2-1} C_{k+p*L} * H_i(k+p*L) * \exp(j*2*\pi*(k+p*L)*i/N). \quad (2.4)$$

For the following analysis it is convenient to assume that the samples at the output of an individual ADC with the number i appear with a frequency F_s and form a sequence $y_i[n]$ that is described by the equations:

$$y_i[n] = x_i[m], \text{ if } n = m*M + i \text{ and} \\ y_i[n] = 0, \text{ otherwise.}$$

The DFT $Y_i[k]$ of the sequence $y_i[n]$ equals:

$$\begin{aligned} Y_i(k) &= \sum_{n=0}^{N-1} y_i[n] * \exp(-j*2*\pi*k/N) = \\ &= \sum_{m=0}^{L-1} x_i[m] * \exp(-j*2*\pi*k*(m*M + i)/N) \\ &= \exp(-j*2*\pi*k*i/N) * \sum_{m=0}^{L-1} x_i[m] * \exp(-j*2*\pi*k*m/L) = \\ &= \exp(-j*2*\pi*k*i/N) * X_i[k]. \end{aligned} \quad (2.5)$$

2.3 The aggregate output.

The output signals of the individual ADC's are combined into an aggregate signal $z[n]$ by interleaving. It is evident that

$$z[n] = \sum_{i=0}^{M-1} y_i[n]. \quad (3.1)$$

Using the equations (3.1), (2.5) and (2.2) the DFT $Z[k]$ of the aggregate output signal $z[n]$ may be presented as:

$$\begin{aligned} Z[k] &= \sum_{i=0}^{M-1} Y_i[k] = \sum_{i=0}^{M-1} \exp(-j*2*\pi*k*i/N) * X_i[k] = \\ &= \sum_{i=0}^{M-1} \exp(-j*2*\pi*k*i/N) * L * \sum_{p=-M/2}^{M/2-1} C_{k+p*L} * H_i(k+p*L) * \exp(j*2*\pi*(k+p*L)*i/N) = \\ &= L * \sum_{p=-M/2}^{M/2-1} C_{k+p*L} * \sum_{i=0}^{M-1} H_i(k+p*L) * \exp(-j*2*\pi*k*i/N) * \exp(j*2*\pi*(k+p*L)*i/N) = \\ &= L * \sum_{p=-M/2}^{M/2-1} C_{k+p*L} * \sum_{i=0}^{M-1} H_i(k+p*L) * \exp(j*2*\pi*p*i/M). \end{aligned} \quad (3.2)$$

2.4 Ideal case: zero misalignment.

When there is no misalignment between the frequency responses of the different AFEs, then all of them have the same transfer function:

$$H_i(k) = H(k) \text{ for all } i, 0 \leq i < M.$$

In that case the DFT $Z[k]$ of the aggregate output signal $z[n]$ becomes:

$$\begin{aligned} Z[k] &= L \sum_{p=-M/2}^{M/2-1} C_{k+p*L} \sum_{i=0}^{M-1} H(k+p*L) \exp(j*2*\pi*p*i/M) = \\ &= L \sum_{p=-M/2}^{M/2-1} C_{k+p*L} H(k+p*L) \sum_{i=0}^{M-1} \exp(j*2*\pi*p*i/M). \end{aligned} \quad (4.1)$$

and after applying the relationship (2.3)

$$Z[k] = L*M*C_k*H(k) = N*C_k*H(k). \quad (4.2)$$

2.5 The transfer functions of the AFEs.

In real life the AFEs are different and therefore the transfer functions $H_i(k)$ are different for different i . One of the transfer functions $H_i(k)$ may be used as a reference transfer function $H_{ref}(k)$. Another way to define the reference transfer function $H_{ref}(k)$ is to average out the transfer functions $H_i(k)$:

$$H_{ref}(k) = 1/M \sum_{i=0}^{M-1} H_i(k).$$

In any case the knowledge of the $H_{ref}(k)$ permits to present the transfer functions $H_i(k)$ in the form:

$$H_i(k) = H_{ref}(k) * (1 + G_i(k)). \quad (5.1)$$

Here the function $G_i(k)$ describes the deviation of the transfer functions $H_i(k)$ from the reference transfer function $H_{ref}(k)$.

2.6 The spurious products.

Substituting the expression (5.1) in the equation (3.2) the DFT $Z[k]$ of the aggregate output signal of the interleaved ADC may be presented as:

$$\begin{aligned} Z[k] &= L \sum_{p=-M/2}^{M/2-1} C_{k+p*L} \sum_{i=0}^{M-1} H_{ref}(k+p*L) * (1 + G_i(k+p*L)) \exp(j*2*\pi*p*i/M) = \\ &= N*C_k*H_{ref}(k) + L \sum_{p=-M/2}^{M/2-1} C_{k+p*L} H_{ref}(k+p*L) \sum_{i=0}^{M-1} G_i(k+p*L) \exp(j*2*\pi*p*i/M). \end{aligned} \quad (6.1)$$

The first term in the last sum describes the DFT $Z_{undistorted}[k]$ of the undistorted aggregate signal at the output of the interleaved ADC:

$$Z_{undistorted}[k] = N*C_k*H_{ref}(k) \quad (6.2)$$

(this expression is similar to the expression (4.2)). The second term in the sum (6.1) describes the DFT $MD(k)$ of the spurious products that appear at the output of the interleaved ADC as a result of misalignment distortions:

$$MD(k) = L \sum_{p=-M/2}^{M/2-1} C_{k+p*L} H_{ref}(k+p*L) \sum_{i=0}^{M-1} G_i(k+p*L) \exp(j*2*\pi*p*i/M). \quad (6.3)$$

2.7 A sine wave as an input signal.

Many of the interleaved ADC features become clear when the input signal is supposed to be a single sine wave:

$$s_a(t) = \sin(2*\pi*k_0*F_s/N*t).$$

In that case the Fourier coefficients C_k of $s_a(t)$ equal zero for all k except $k = k_0$ and $k = -k_0$ with the relationship $C_{-k_0} = C_{k_0}^*$. The coefficients C_{k+pL} in the expression (6.3) differ from zero only if

$$\begin{aligned} k + pL &= k_0, \text{ or} \\ k + pL &= -k_0, \end{aligned} \quad (7.1)$$

so that the spurious components appear at the frequencies $k = \pm k_0 - pL$, $-M/2 \leq p < M/2$. The amplitude of the spurious component with the frequency $k_0 - pL$ equals

$$MD(k_0 - pL) = L * C_{k_0} * H_{ref}(k_0) * \sum_{i=0}^{M-1} G_i(k_0) * \exp(j * 2 * \pi * p * i / M).$$

With the designation

$$g(k_0, p) = \sum_{i=0}^{M-1} G_i(k_0) * \exp(j * 2 * \pi * p * i / M)$$

the last equation becomes

$$MD(k_0 - pL) = L * C_{k_0} * H_{ref}(k_0) * g(k_0, p).$$

The mean square root value $SpursRMS$ of the sum of the spurious components equals

$$SpursRMS = \sqrt{\sum_{p=-M/2}^{M/2-1} MD(k_0 - pL)^2} = L * C_{k_0} * H_{ref}(k_0) * \sqrt{\sum_{p=-M/2}^{M/2-1} g(k_0, p)^2}$$

According to the Parseval's theorem

$$\sum_{p=-M/2}^{M/2-1} g(k_0, p)^2 = M * \sum_{i=0}^{M-1} G_i(k_0)^2.$$

Therefore the mean square root value $SpursRMS$ of the sum of the spurious components equals

$$SpursRMS = L * C_{k_0} * H_{ref}(k_0) * \sqrt{M * \sum_{i=0}^{M-1} G_i(k_0)^2}.$$

The signal to noise and distortions ratio $SINAD$ may be found by dividing the magnitude of the undistorted signal (6.2) by the spurious components overall mean square root value $SpursRMS$:

$$\begin{aligned} SINAD &= Z_{undistorted}[k] / SpursRMS = \\ &= \sqrt{M} / \sqrt{\sum_{i=0}^{M-1} G_i(k_0)^2} \end{aligned} \quad (7.4)$$

The spurious-free dynamic range $SFDR$ may be found through $SINAD$ as:

$$SFDR = 20 * \lg(SINAD) \quad (7.5)$$

Accordingly

$$ENOB = (SFDR - 1.76) / 6.02 \quad (7.6)$$

2.8 The description of the Analog Front Ends misalignment.

The deviation of the transfer functions $H_i(k)$ from the reference transfer function $H_{ref}(k)$ may be described with the use of the usual concepts of loss and phase shift.. The deviations of the loss $\Delta b_i(k)$ and the phase shift $\Delta \varphi_i(k)$ from the reference values for the AFE with the number i are defined in the natural way:

$$\begin{aligned} \Delta b_i(k) &= 20 \lg H_i(k) / H_{ref}(k), \\ \Delta \varphi_i(k) &= \arg (H_i(k) / H_{ref}(k)). \end{aligned} \quad (8.1)$$

It follows from these definitions that the module of the transfer functions $H_i(k)$ equals:

$$H_i(k) = H_{\text{ref}}(k) * \exp(\ln 10/20 * \Delta b_i(k))$$

or, since $\ln 10/20 = 0.1151$,

$$H_i(k) = H_{\text{ref}}(k) * \exp(0.1151 * \Delta b_i(k)).$$

The transfer functions $H_i(k)$ itself equals:

$$H_i(k) = H_{\text{ref}}(k) * \exp(0.1151 * \Delta b_i(k)) * \exp(j * \Delta \varphi_i(k)).$$

Since the deviations Δb_i and $\Delta \varphi_i$ are small enough, the expression for the transfer functions $H_i(k)$ may be rewritten in the form:

$$H_i(k) = H_{\text{ref}}(k) * (1 + 0.1151 * \Delta b_i(k) + j * \Delta \varphi_i(k)),$$

So that the function $G_i(k)$, that was used above for description of the difference between the AFE with the number i and the reference AFE, equals:

$$G_i(k) = 0.1151 * \Delta b_i(k) + j * \Delta \varphi_i(k). \quad (8.2)$$

The signal to noise and distortions ratio SINAD (7.4) after a substitution of the equation (8.2) becomes

$$\text{SINAD} = \sqrt{M} / \sqrt{\sum_{i=0}^{M-1} (0.1151 * \Delta b_i(k_0) + j * \Delta \varphi_i(k_0))^2} \quad (8.3)$$

2.9 Average deviations.

Another way to describe the misalignments between different AFEs as a whole is to define average deviation of the loss $\Delta b(k)$ and average deviation of the phase shift $\Delta \varphi(k)$ by the next expressions:

$$\Delta b(k) = \sqrt{(1/M * \sum_{i=0}^{M-1} (\Delta b_i(k))^2)}. \quad (9.1)$$

$$\Delta \varphi(k) = \sqrt{(1/M * \sum_{i=0}^{M-1} (\Delta \varphi_i(k))^2)}. \quad (9.2)$$

Then the part of SINAD that is caused by the loss deviation equals:

$$\text{SINAD}_b = 1 / (0.1151 * \Delta b(k_0)) \quad (9.3)$$

and the part of SINAD that is caused by the phase shift deviation equals:

$$\text{SINAD}_{\Delta \varphi} = 1 / \Delta \varphi(k_0).$$

The correspondent expressions for the spurious-free dynamic range SFDR and the effective number of bits ENOB, that are caused by the loss deviation and the phase shift deviation, appear as:

$$\text{SFDR}_b = -20 * \lg(0.1151 * \Delta b(k_0)). \quad (9.4)$$

$$\begin{aligned} \text{SFDR}_{\Delta \varphi} &= -20 * \lg(\Delta \varphi(k_0)). \\ \text{ENOB}_b &= (-20 * \lg(0.1151 * \Delta b(k_0)) - 1.76) / 6.02. \end{aligned} \quad (9.5)$$

$$\text{ENOB}_{\Delta \varphi} = (-20 * \lg(\Delta \varphi(k_0)) - 1.76) / 6.02.$$

The equations (9.4) and (9.5) were used to calculate the relationship between the loss mismatch $\Delta b(k)$ and phase shift mismatch $\Delta \varphi(k)$ on the one hand and the SFDR and ENOB on the other hand under the condition that sine wave at the input of the interleaved ADC has the correspondent frequency $f = k_0 * F_s / N$. The calculation results are shown in Fig.3, Fig.4, Fig.5 and Fig.6.

2.10 An Example.

It may be seen from the Fig.2.3 and Fig.2.5, that to achieve ENOB in the neighborhood of 5-5.5 bits, it is necessary to reduce the misalignment of the frequency responses to about 0.2 dB in the loss mismatch and 0.02 rad in the phase shift mismatch. For the input frequency 10 GHz the phase shift of 0.02 rad corresponds to delay of approximately 0.3 ps.

3 The Time Variant Equalizer.

The block diagram of the time variant equalizer (TVE) is shown in the Fig.3.1 [4]. The TVE is able to work in two modes: in a calibration mode and in an operational mode. In the calibration mode the measurement unit receives the signal from calibrator signal generator (see Fig.1) measures the frequency response of each individual ADC with the analog front end AFE. The frequency response of the pair ADC-AFE with the number i is used as a source for calculation of the i -th set of the TVE coefficients $C_{i0}, C_{i1}, \dots, C_{i,EL-1}$, $0 \leq i < M$ (EL is the equalizer length, i.e. the number of taps in the equalizer inner shift register). The whole assembly of M sets of the TVE coefficients is loaded into coefficients memory through the memory load bus, the i -th set of the TVE coefficients being placed into the memory area with an address prefix that equals the number i . In the operational mode the clock advances the M counter making it to go through the stages 0, 1, ..., $M-1$, 0, .. and so on. The number i of the stage goes from the M counter to the coefficients memory through the address bus, so that the i -th set of the TVE coefficients $C_{i0}, C_{i1}, \dots, C_{i,EL-1}$ appear on the coefficients bus. The samples from the interleaver output come to the TVE input and are clocked in the shift register. The M counter is synchronized with interleaver operation so, that the counter transits into the stage i when the sample from the i -th individual ADC comes to the TVE input. The multipliers together with the adder form a convolution sum of the last group of EL samples, that have come to the TVE input from the interleaver, with the the i -th set of the TVE coefficients. Consequently, the transfer function of the TVE varies in time with every change of the M counter stage, the pulse response of the TVE at some time instant being equal to the set $C_{i0}, C_{i1}, \dots, C_{i,EL-1}$, where i is the current stage of the M counter. The assembly of M sets of the TVE coefficients $C_{i0}, C_{i1}, \dots, C_{i,EL-1}$, $0 \leq i < M$, is calculated in the calibration mode in such a way, that the frequency response of the i -th pair ADC-AFE is corrected. The operation of the TVE as a whole ensures equalization of the misalignment deviations between the frequency responses of the different ADC-AFE.

4 Experimental Results

The equalization technology has been used with different types of digitizers built with multiple interleaved ADCs. Below there are some experimental results.

4.1 3GHz, 8Gbits/s, 10-bit Digitizer

This digitizer uses four interleaved ADCs AT84AS004 from E2V to achieve sampling rate of 8 Gbits/s. FFT of the acquired data for the input signal 2.47 GHz with -3dBFS level is shown in the Fig.4.1. The misalignment in the high frequency part of the input signal creates the following major spur components:

$$\begin{aligned} f_{\text{clk}}/2 - f_{\text{signal}} &= 4 \text{ GHz} - 2.47 \text{ GHz} = 1.53 \text{ GHz} \\ f_{\text{clk}}/4 - f_{\text{signal}} &= 2 \text{ GHz} - 2.47 \text{ GHz} = -0.47 \text{ GHz} \text{ (reflected component)} \\ 3 * f_{\text{clk}}/4 - f_{\text{signal}} &= 6 \text{ GHz} - 2.47 \text{ GHz} = 3.53 \text{ GHz}. \end{aligned}$$

Since the levels of these components are relatively high they substantially affect the SFDR and ENOB of the digitizer.

The FFT of the same signal with digital equalizer for amplitude and group delay is shown in Fig 4.2. The level of spur components is significantly reduced.

4.2 3GHz, 12Gbit/s, 8-bit Digitizer

This digitizer used four interleaved ADC 083000 from National semiconductor. Fig 4.3 shows ENOB (with equalizer) versus frequency for input level -6dBFS . For comparison, the ENOB of ADC chip itself is shown on the same graph. The ENOB of digitizer is lower than ADC itself in low frequency area because noise impact of front end with amplification about 15dB.

In high frequency area situation is different. ENOB of digitizer is higher compared with ADC itself because equalizer reduces misalignment between two ADC inside of each ADC chip. Fig 4.4 shows how ENOB is changed with equalizer and equalizer combined with digital filter 3GHz. As before, major impact of equalizer can be observed at high frequency. The digital filter increases ENOB mostly because off-band noise suppression.

4.3 8 GHz/20 Gs/s 8-bit Digitizer

This digitizer is built with proprietary ADC chip with multiple interleaved ADCs with aggregate sampling rate of 20 Gs/s. FFT of acquired signal of 5.132 GHz with level about -1 dBFS is shown in Fig 4.5 without equalizer and in Fig 4.6 with the equalizer. It can be seen that the amplitude of most of the spur components is significantly reduced. Particularly significant spur components of the following frequencies:

$$\begin{aligned} f_{\text{clk}}/2 - f_{\text{signal}} &= 10\text{ GHz} - 5.132\text{ GHz} = 4.868\text{ GHz} \\ f_{\text{clk}}/5 - f_{\text{signal}} &= 4\text{ GHz} - 5.132\text{ GHz} = -1.132\text{ GHz (reflected component)} \\ 9*f_{\text{clk}}/20 - f_{\text{signal}} &= 9\text{ GHz} - 5.132\text{ GHz} = 3.868\text{ GHz} \\ f_{\text{clk}} - (9*f_{\text{clk}}/20 + f_{\text{signal}}) &= 20\text{ GHz} - 14.132\text{GHz} = 5.868\text{ GHz}. \end{aligned}$$

The spur component $f_{\text{clk}}/2 - f_{\text{signal}}$ is reduced from -40.9 dBFS to -65.9 dBFS . The side band from the third harmonic of the signal with the frequency $20\text{ GHz} - 15.39\text{ GHz} = 4.6\text{ GHz}$ has the same amplitude with and without the equalizer as a result of the non-linear distortions. Fig 4.7 shows ENOB versus frequency with and without equalizer. Fig 4.8 shows SFDR versus frequency with and without equalizer.

4.4 13 GHz, 40 Gs/s, 8-bit Digitizer

This digitizer is built with two interleaved ADC chips as in paragraph 4.3. FFT of acquired signal of 7.132 GHz with level about -1dBFS is shown in Fig 4.9 without equalizer, and in Fig 4.10 with equalizer. As before the reduction of most of the spur components can be seen. As an example the amplitude reduction of spur component with frequency $f_{\text{clk}}/4 - f_{\text{signal}} = 10\text{ GHz} - 7.132\text{ GHz} = 2.868\text{ GHz}$ increases SFDR from 38 dBc to 48 dBc. ENOB versus frequency and SFDR versus frequency are shown in Fig.4.11 and Fig.4.12 respectively.

5 Conclusion

The digital equalizer is a powerful tool to improve the performance of interleaved ADC. It can not only reduce mismatch in amplitude and grope delay frequency responses, but also equalizes this frequency response to the required target. Fig 5.1 shows the equalized frequency response of the 13 GHz/40 Gs/s and 8 GHz/20Gs/s digitizers. 6th order Butterworth response with linear group delay has been used as an equalization target. The step response after equalization is shown in Fig 5.2 for the 8 GHz/20Gs/s digitizer and in Fig.5.3 for the 13 GHz/40 Gs/s digitizer.

6 References

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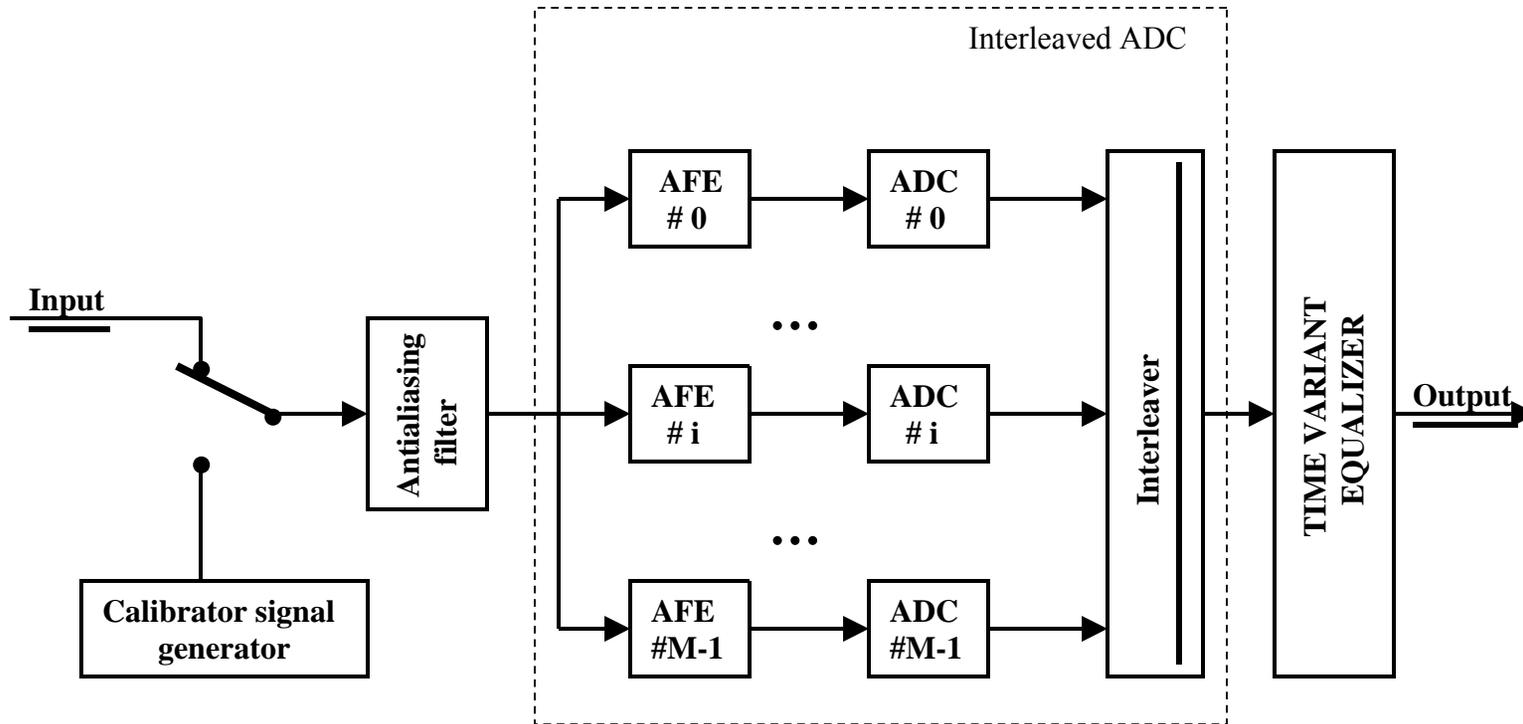


Figure 1.1 Interleaved Digitizer

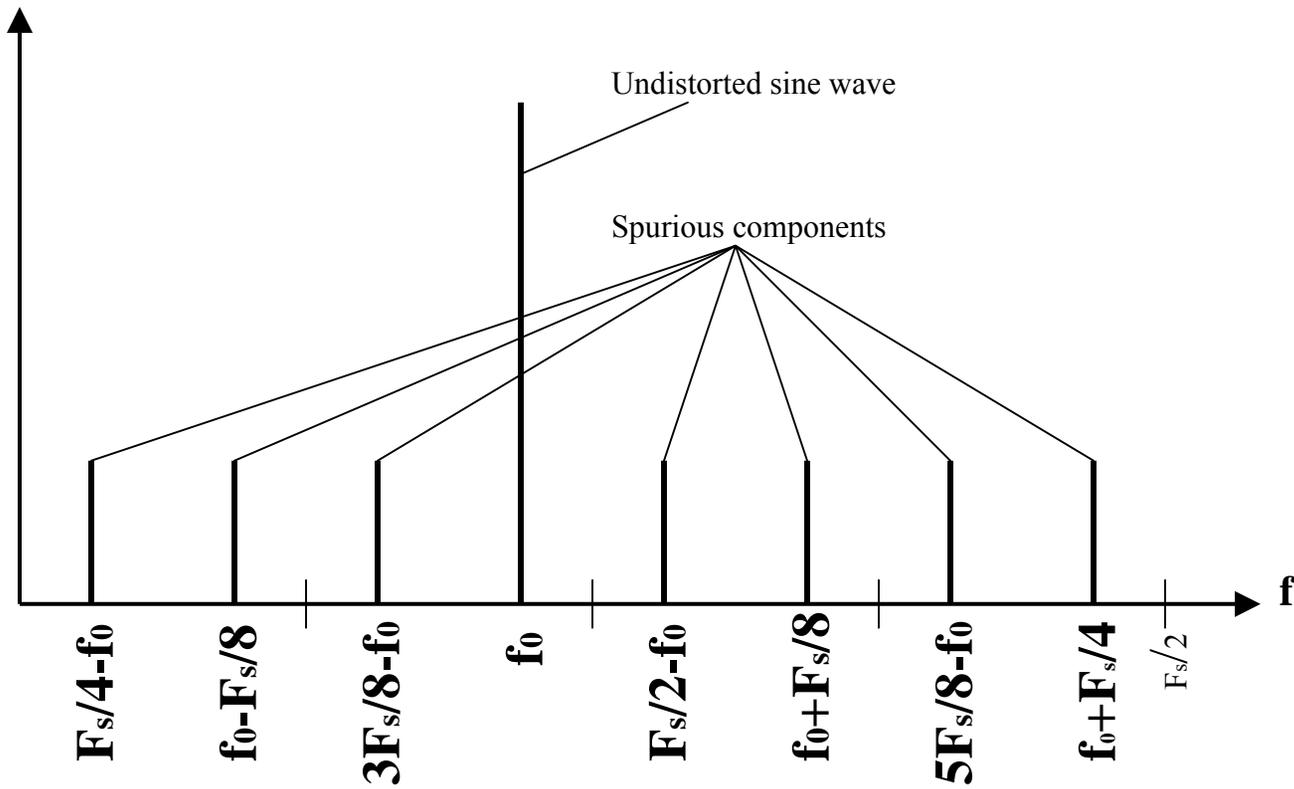


Figure 2.1 Output Spectrum of 8 Interleaved ADCs



Figure 2.2 SFDR vs. Loss Mismatch

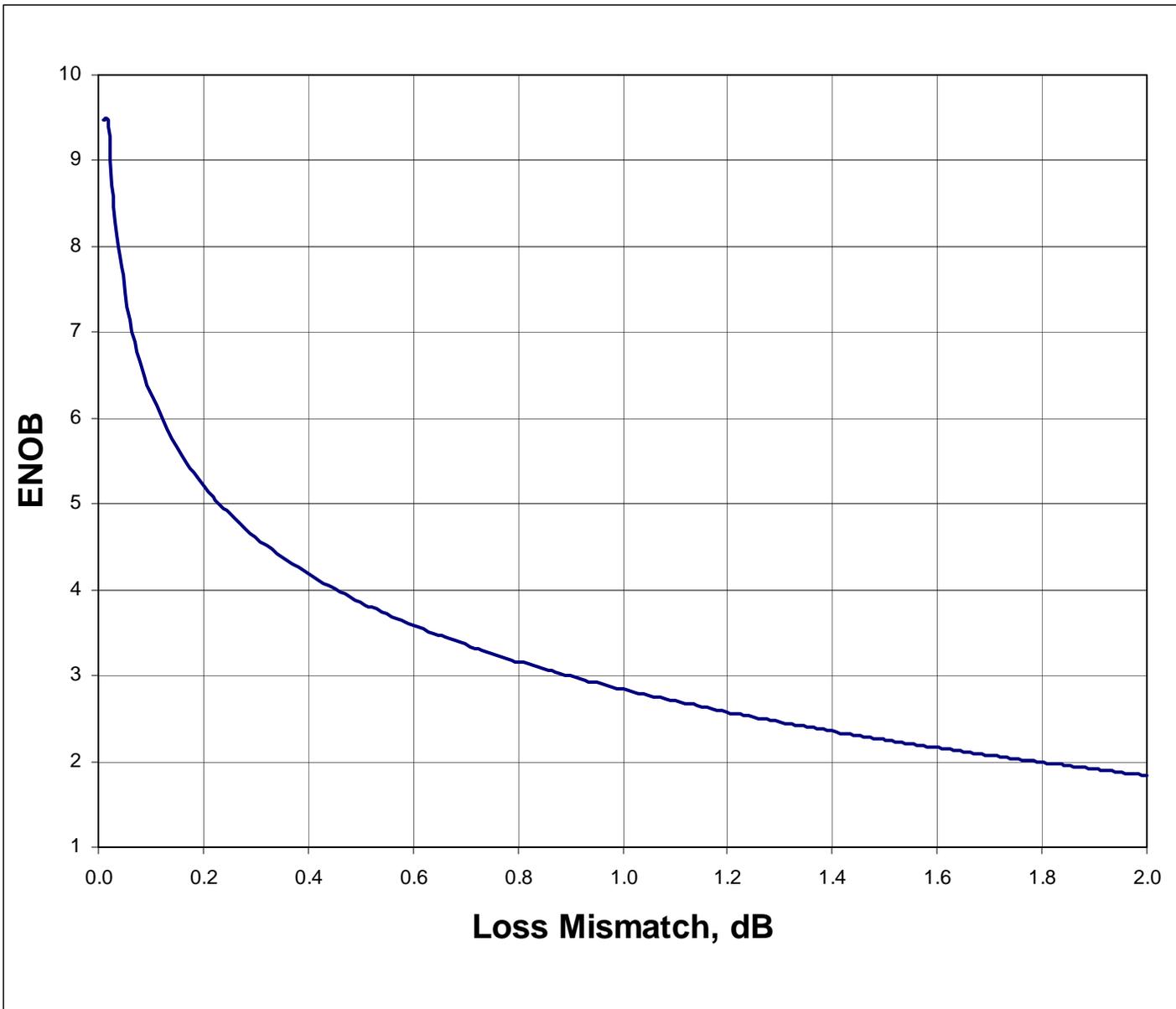


Figure 2.3 ENOB vs. Loss Mismatch

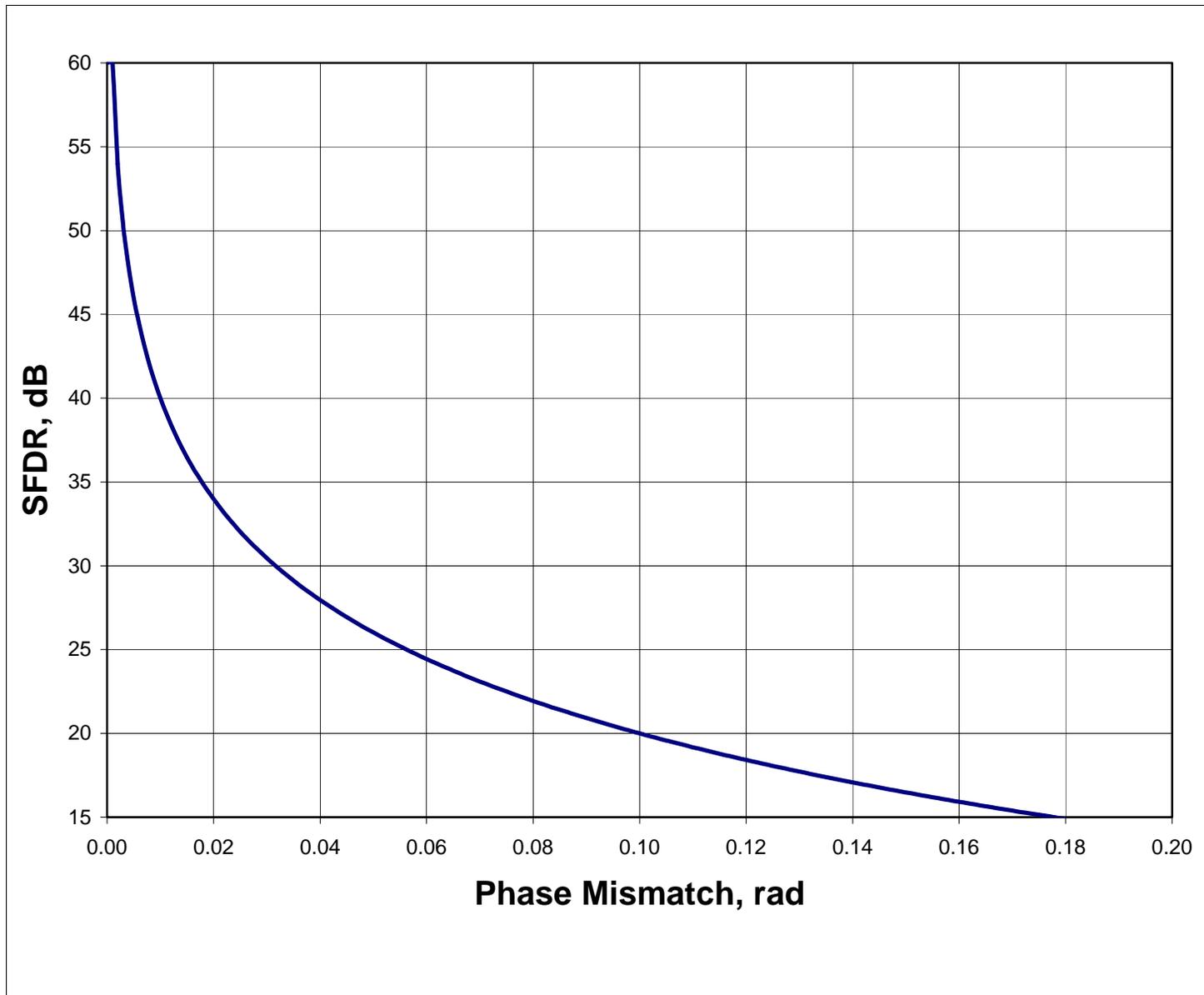


Figure 2.4 SFDR vs. Phase Mismatch



Figure 2.5 ENOB vs. Phase Mismatch

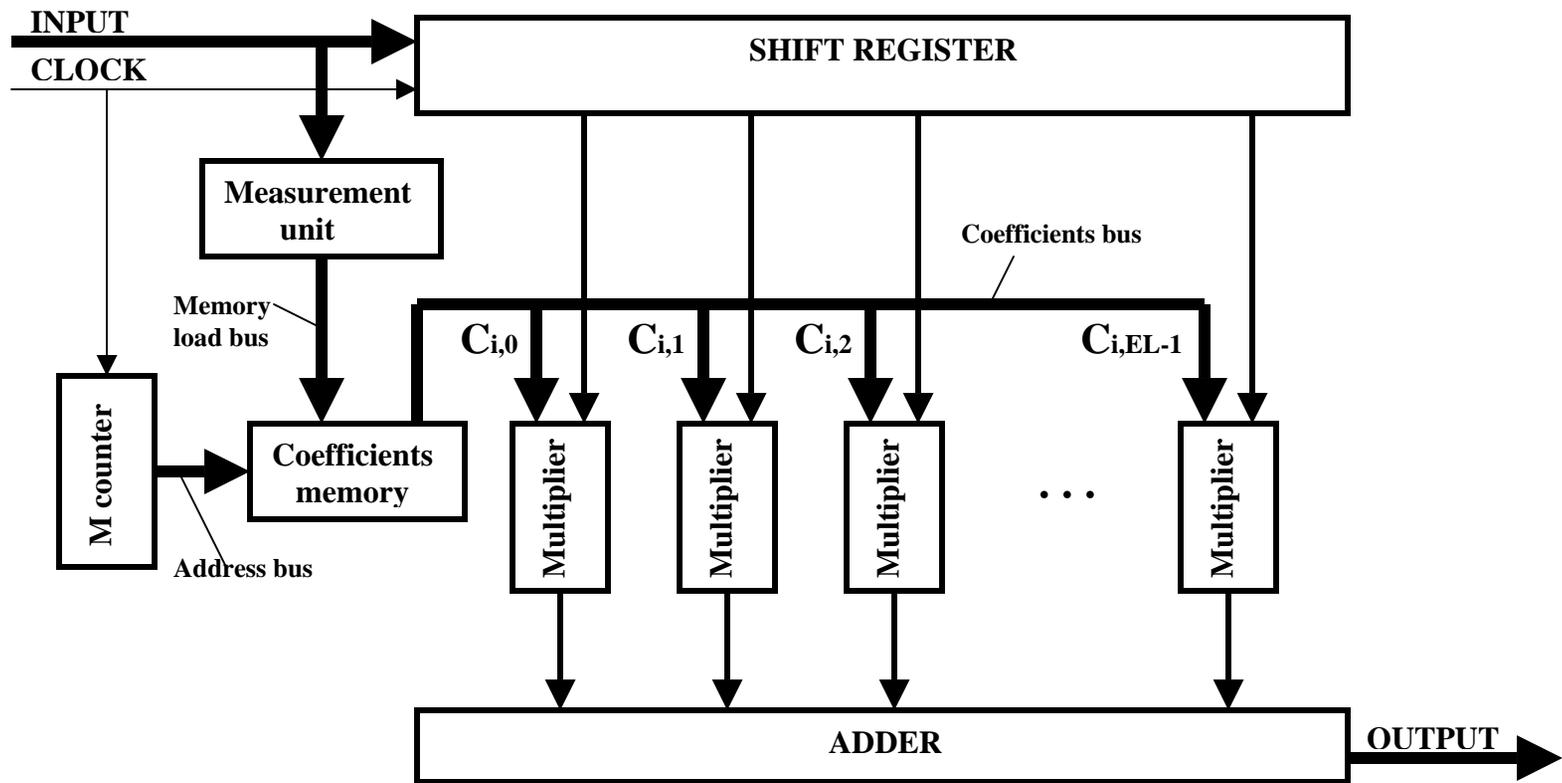
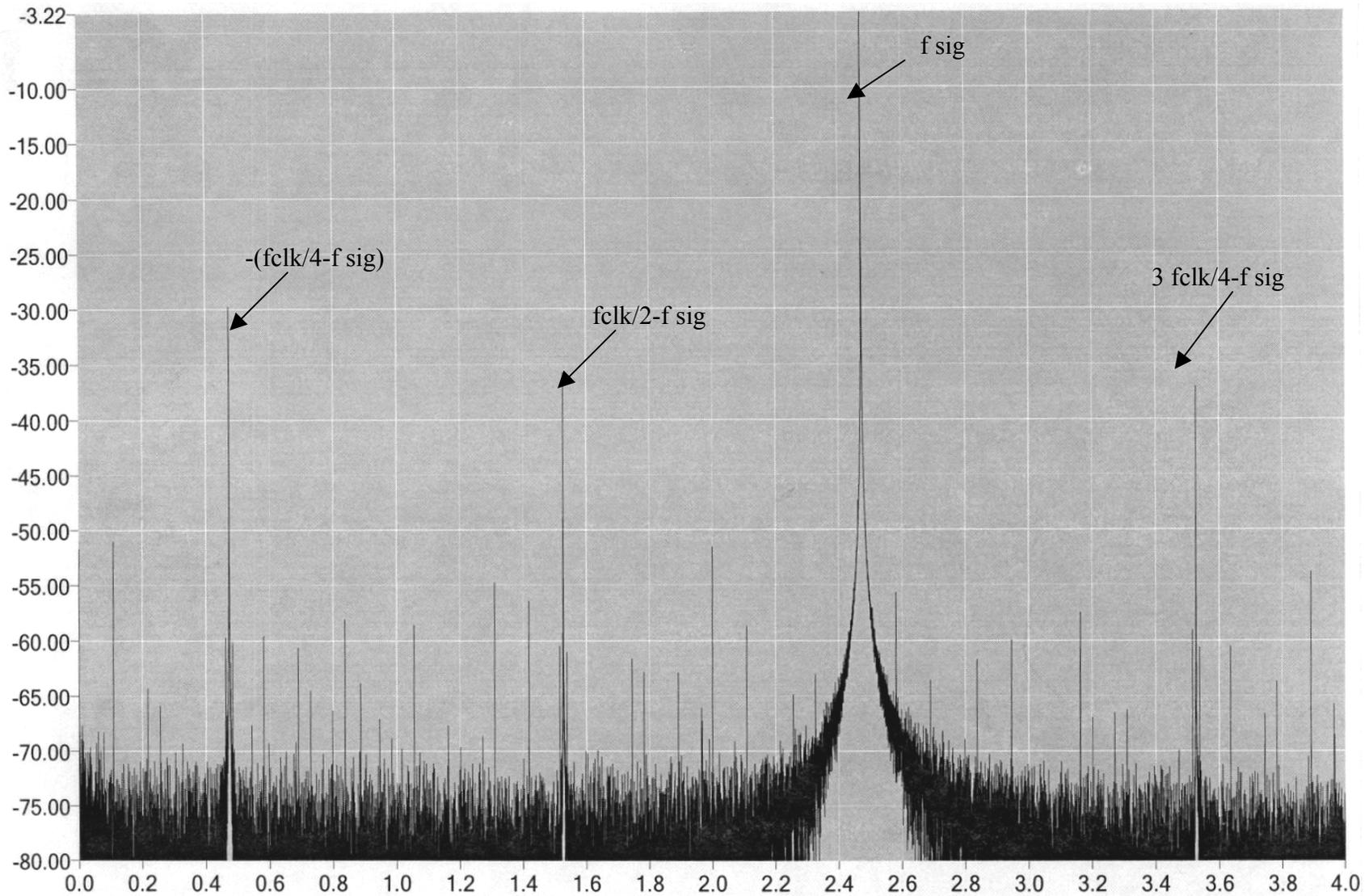


Figure 3.1 Time Variant Equalizer



**Figure 4.1 3 GHz, 8Gs/s, 10-bit digitizer
FFT of Acquired Signal, 2.47 GHz**

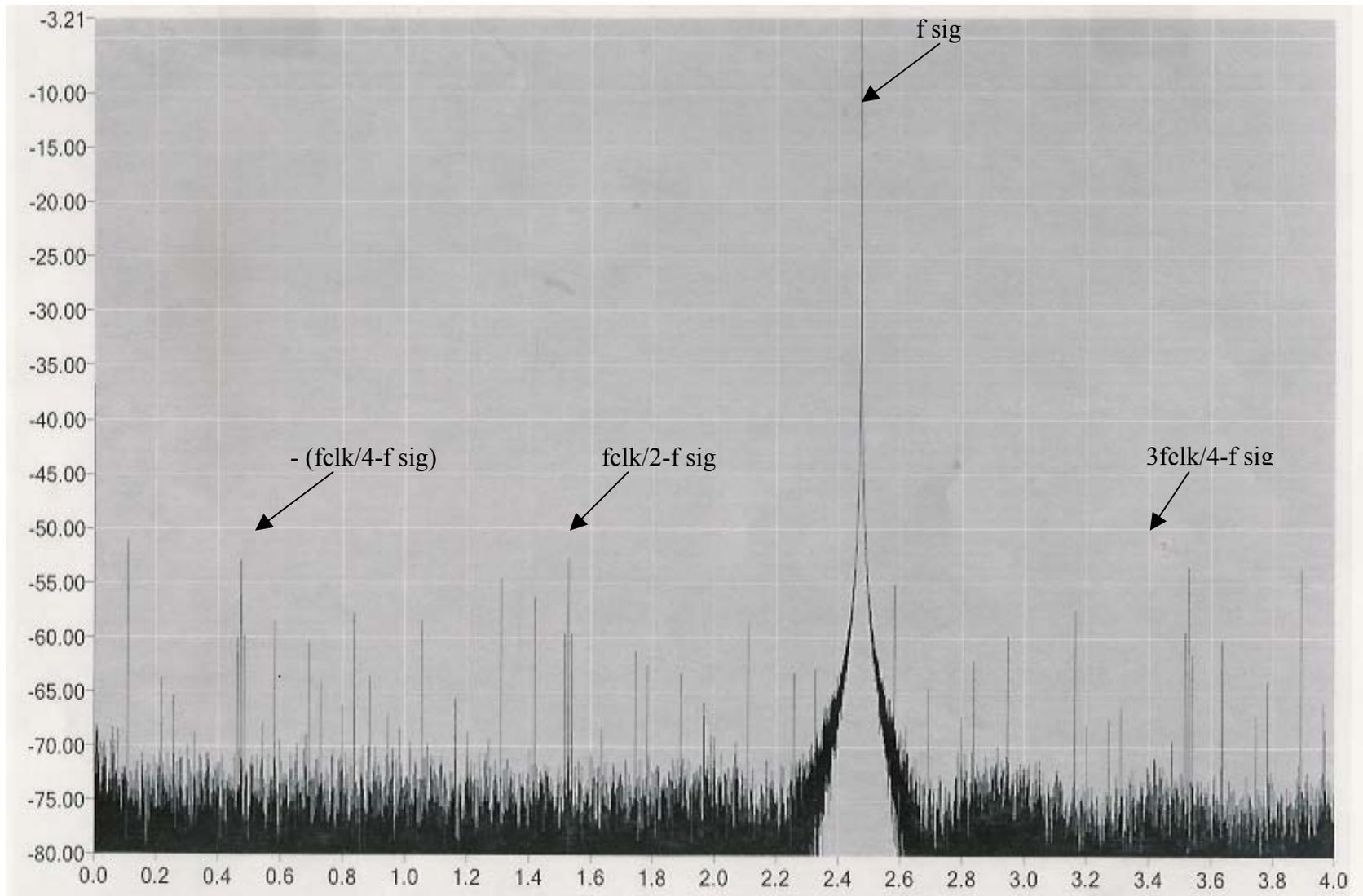
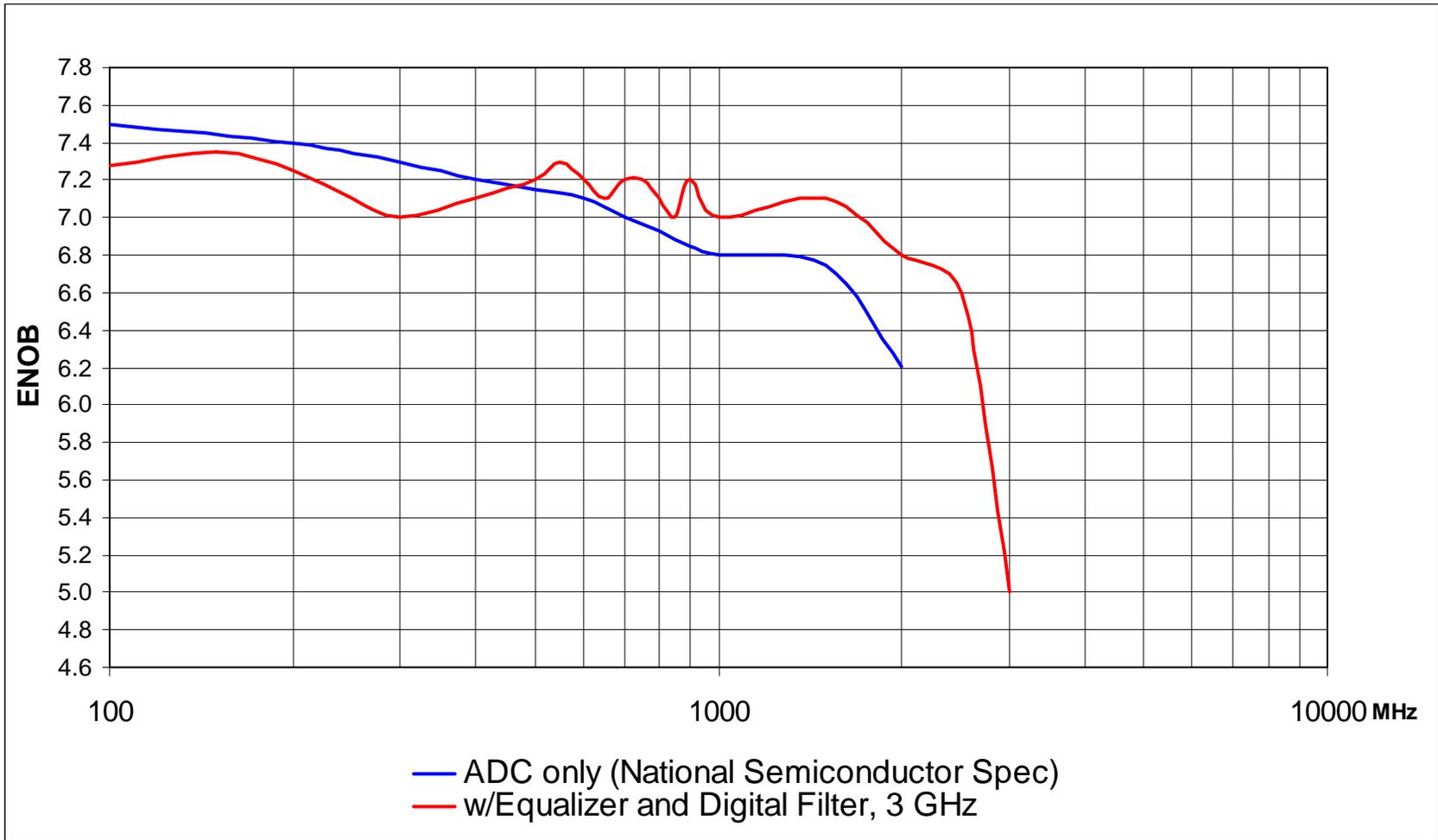
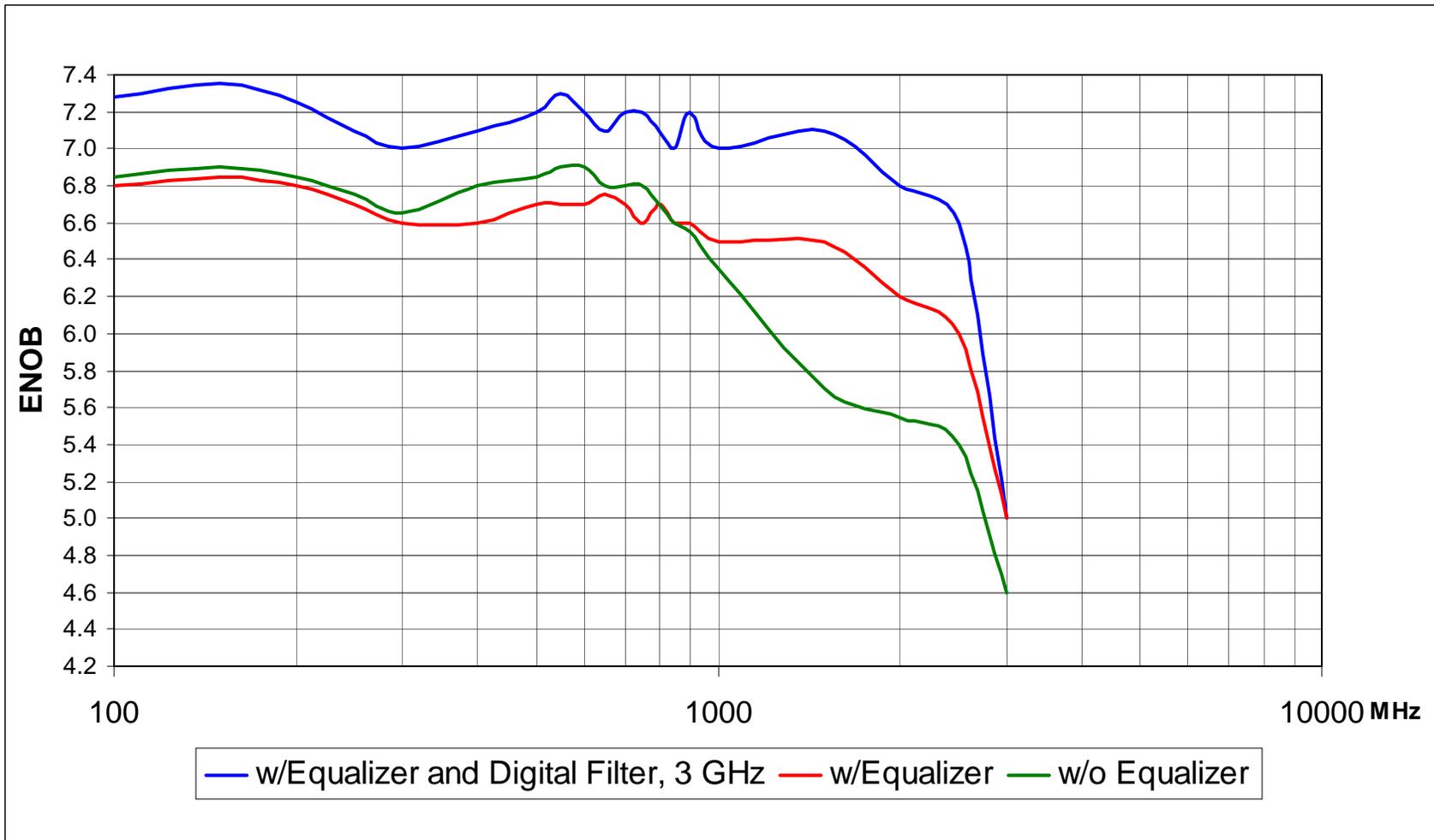


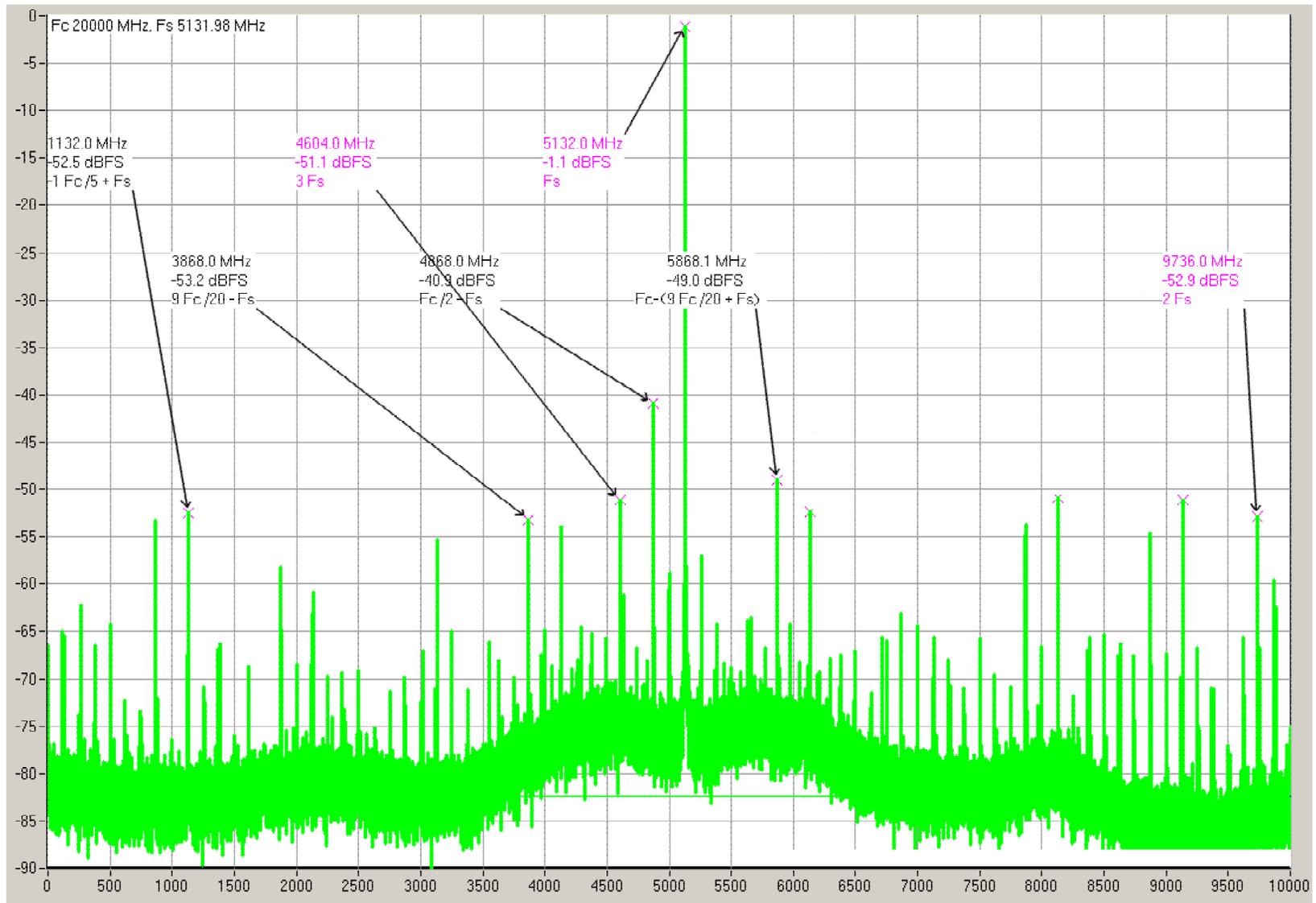
Figure 4.2 Same as Figure 4.1, But With Digital Equalizer



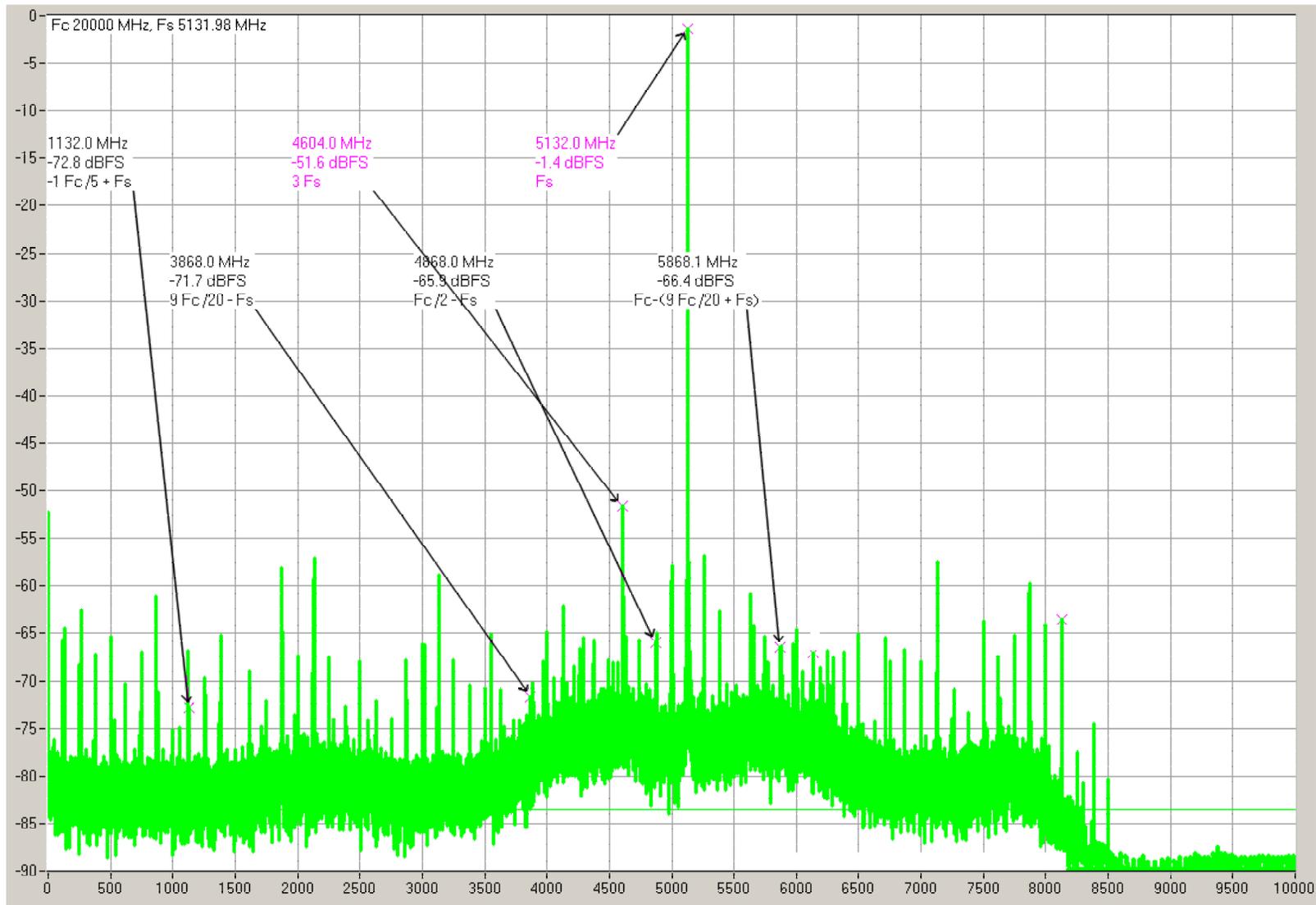
**Figure 4.3 3Ghz, 12Gbit/s, 8-Bit Digitizer
ENOB vs. Frequency**



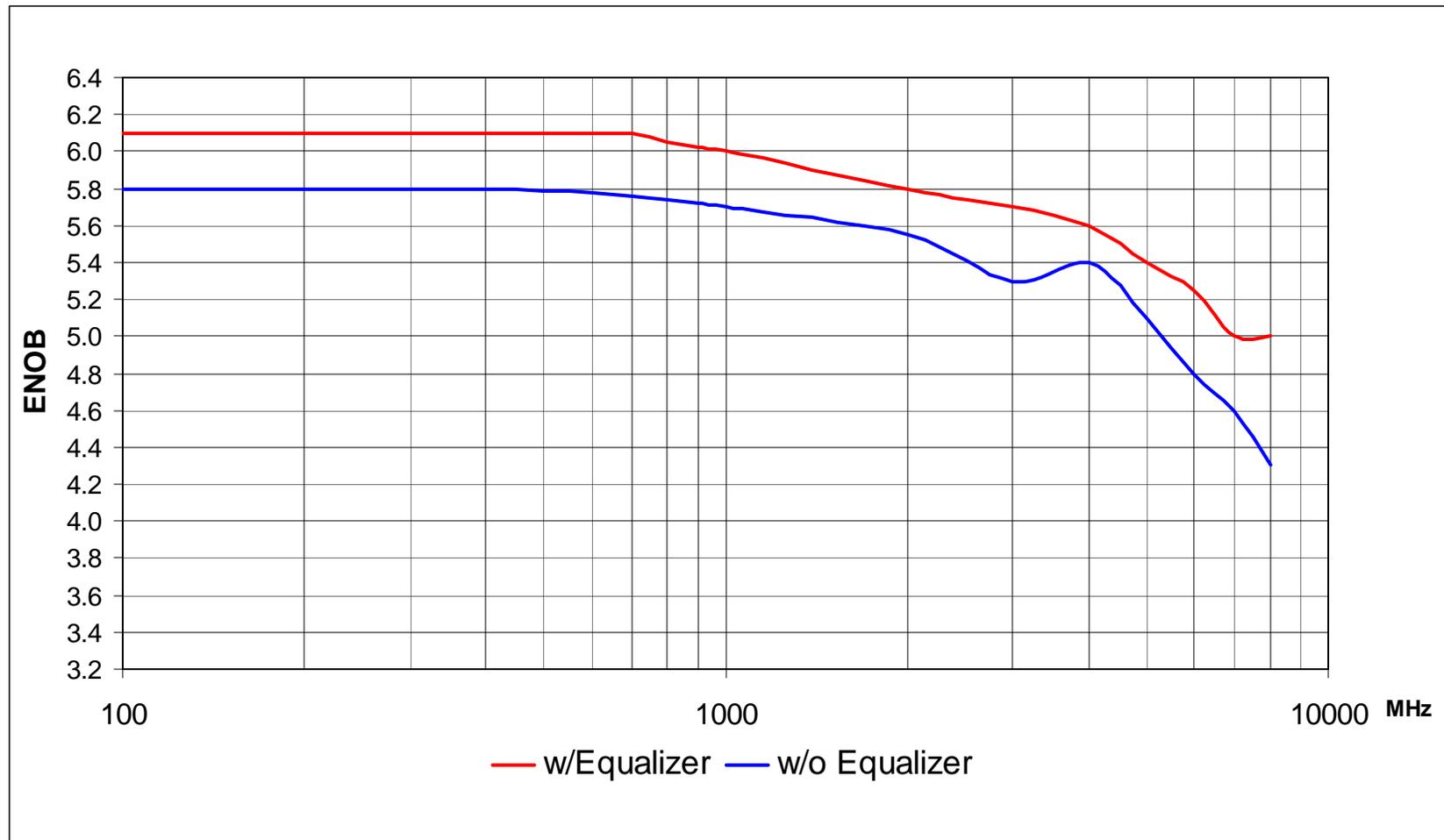
**Figure 4.4 3Ghz, 12Gbit/s, 8-Bit Digitizer
ENOB vs. Frequency**



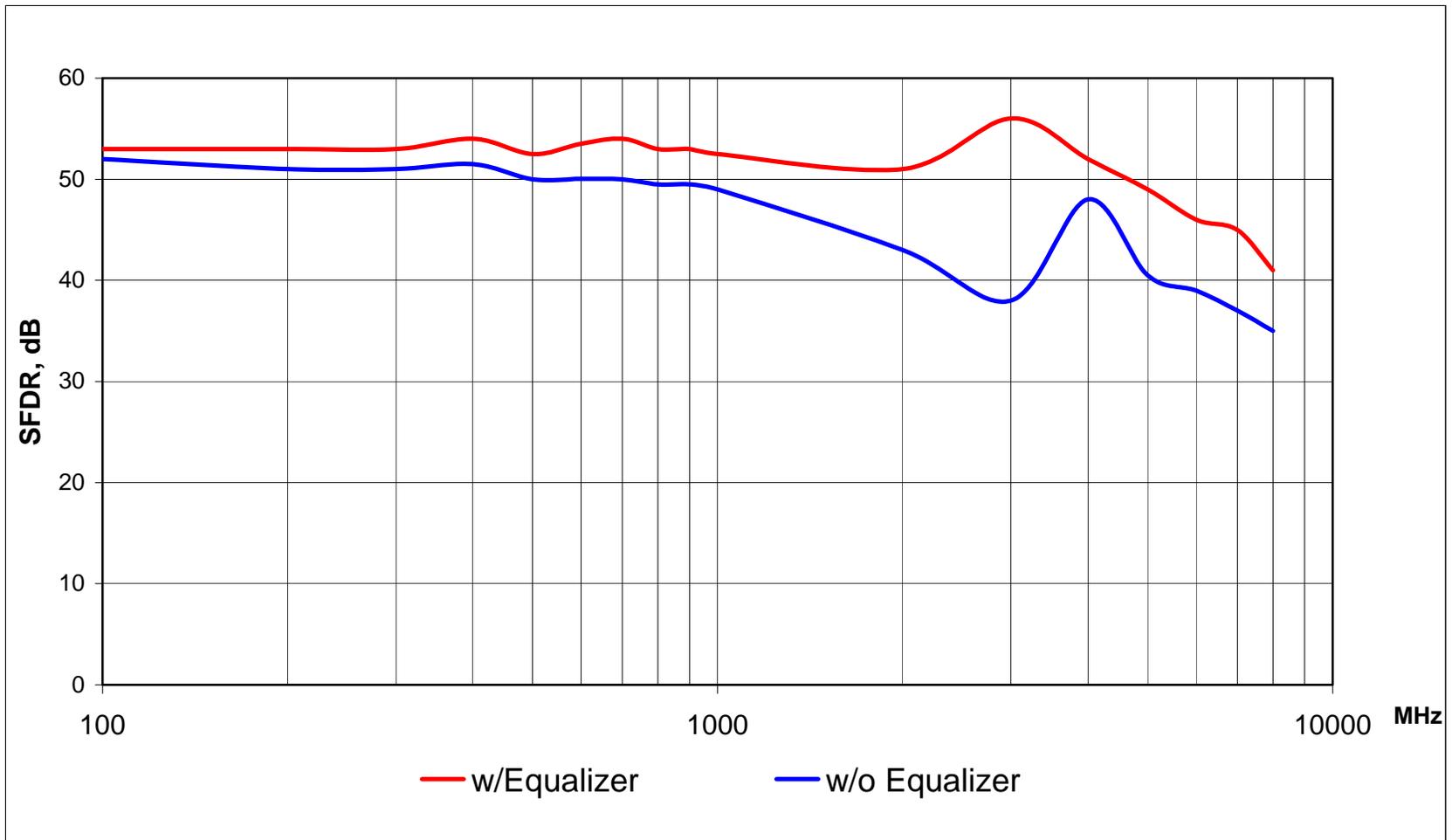
**Figure 4.5 8GHz, 20Gs/s, 8-bit Digitizer
FFT of Acquired Signal 5.132GHz, No Equalizer**



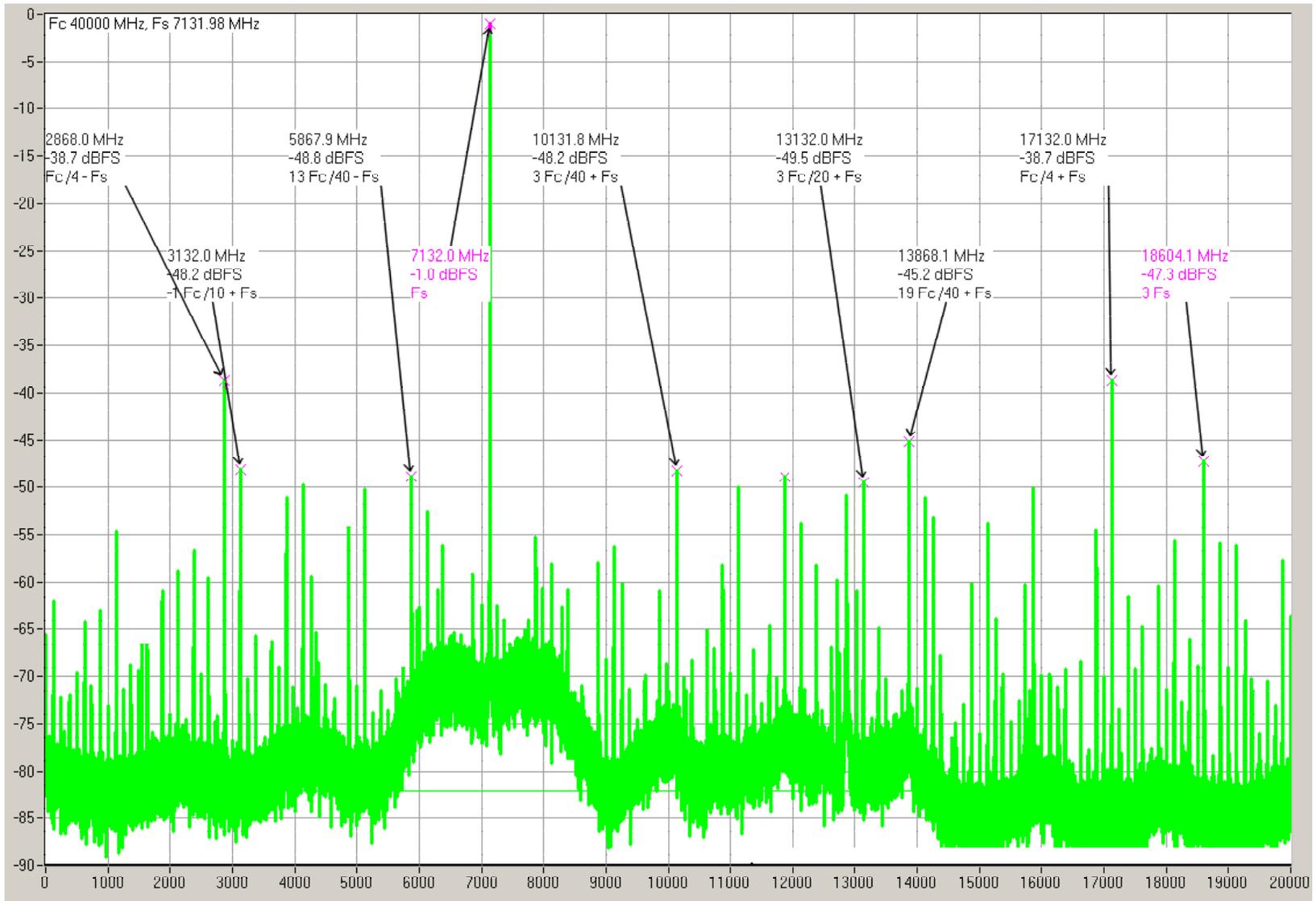
**Figure 4.6 Same as Figure 4.5
With Equalizer and Digital Filter, 8GHz**



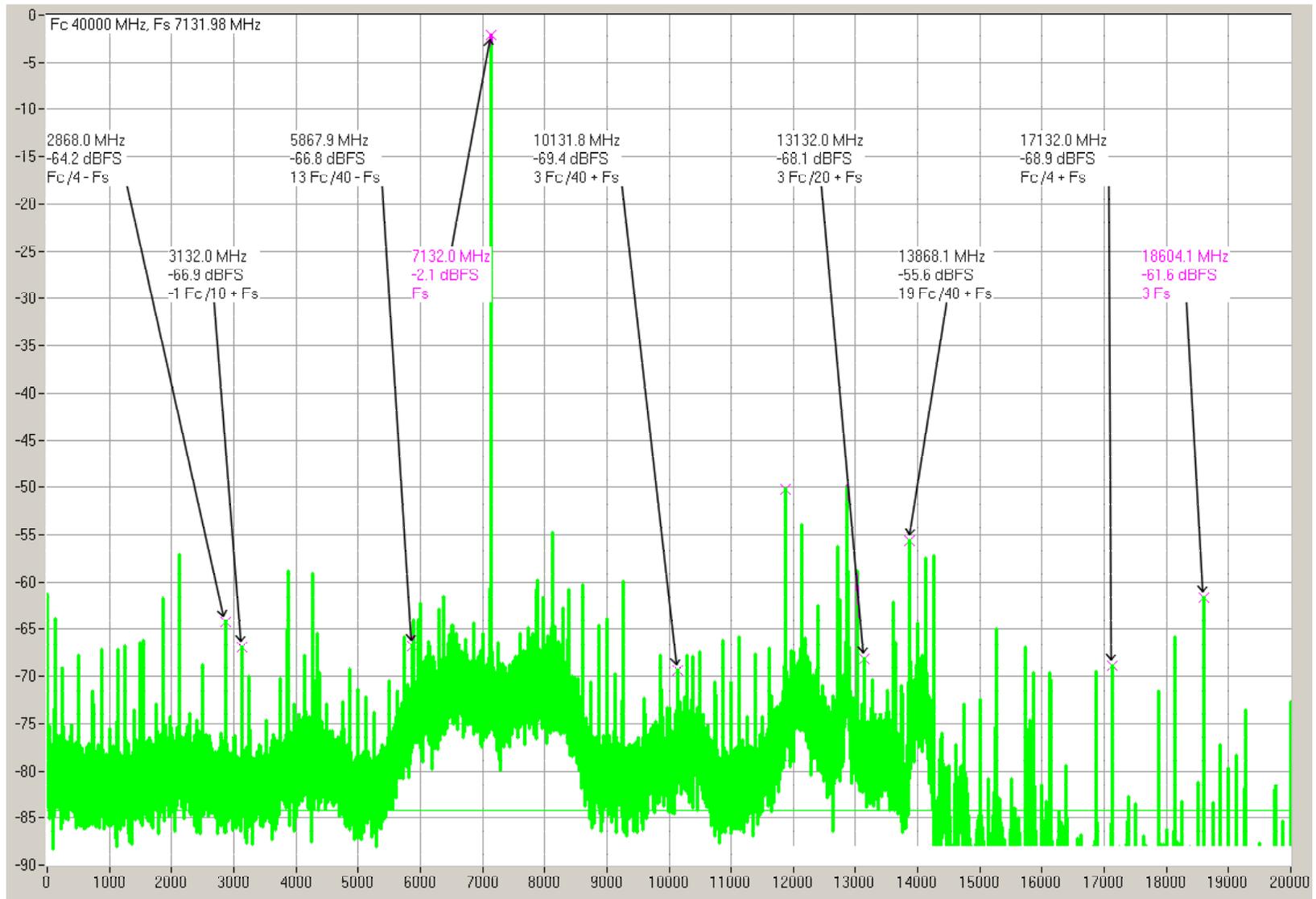
**Figure 4.7 8Ghz, 20Gbit/s, 8-Bit Digitizer
ENOB vs. Frequency**



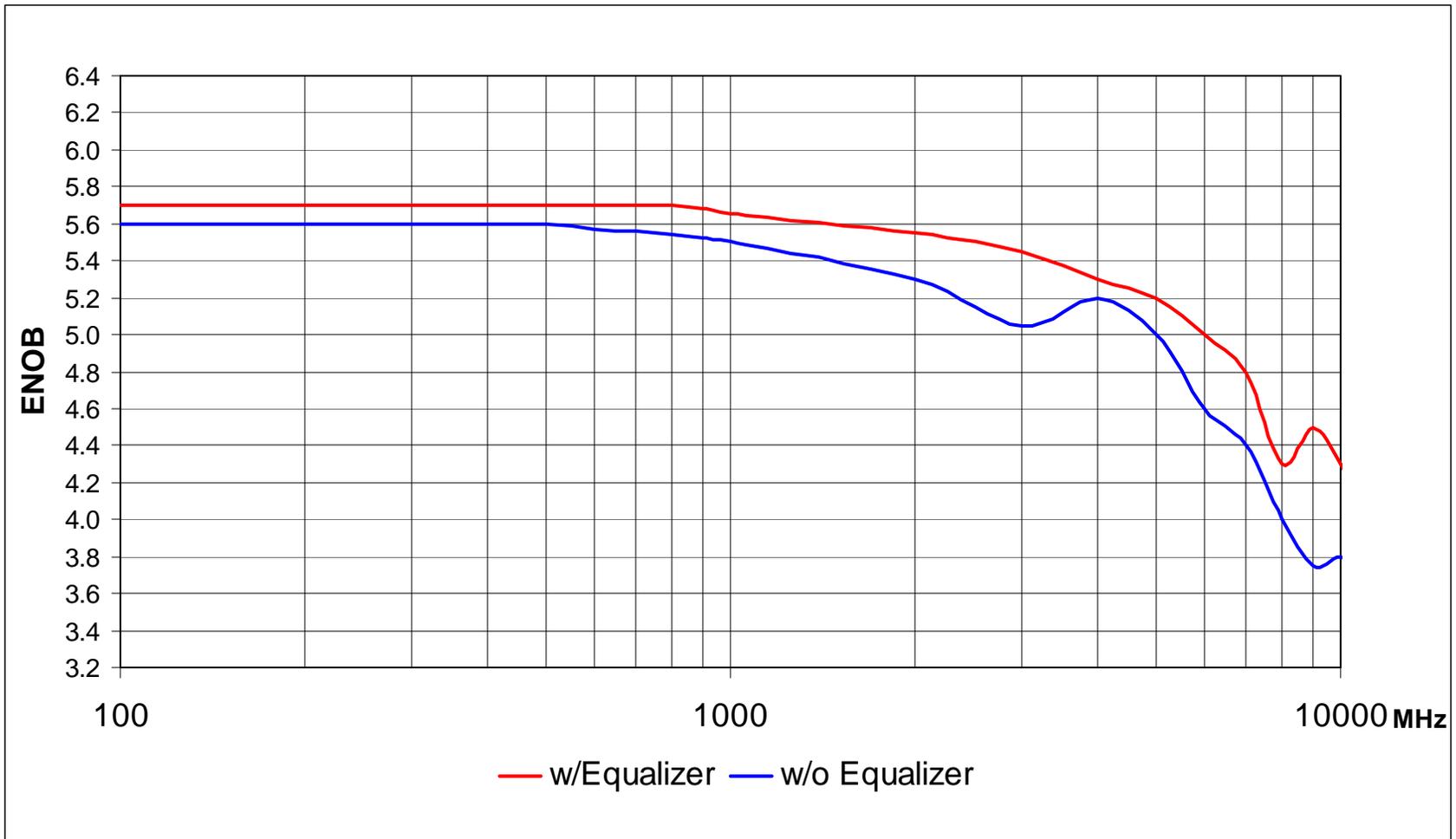
**Figure 4.8 8GHz, 20Gbit/s, 8-Bit Digitizer
SFDR vs. Frequency**



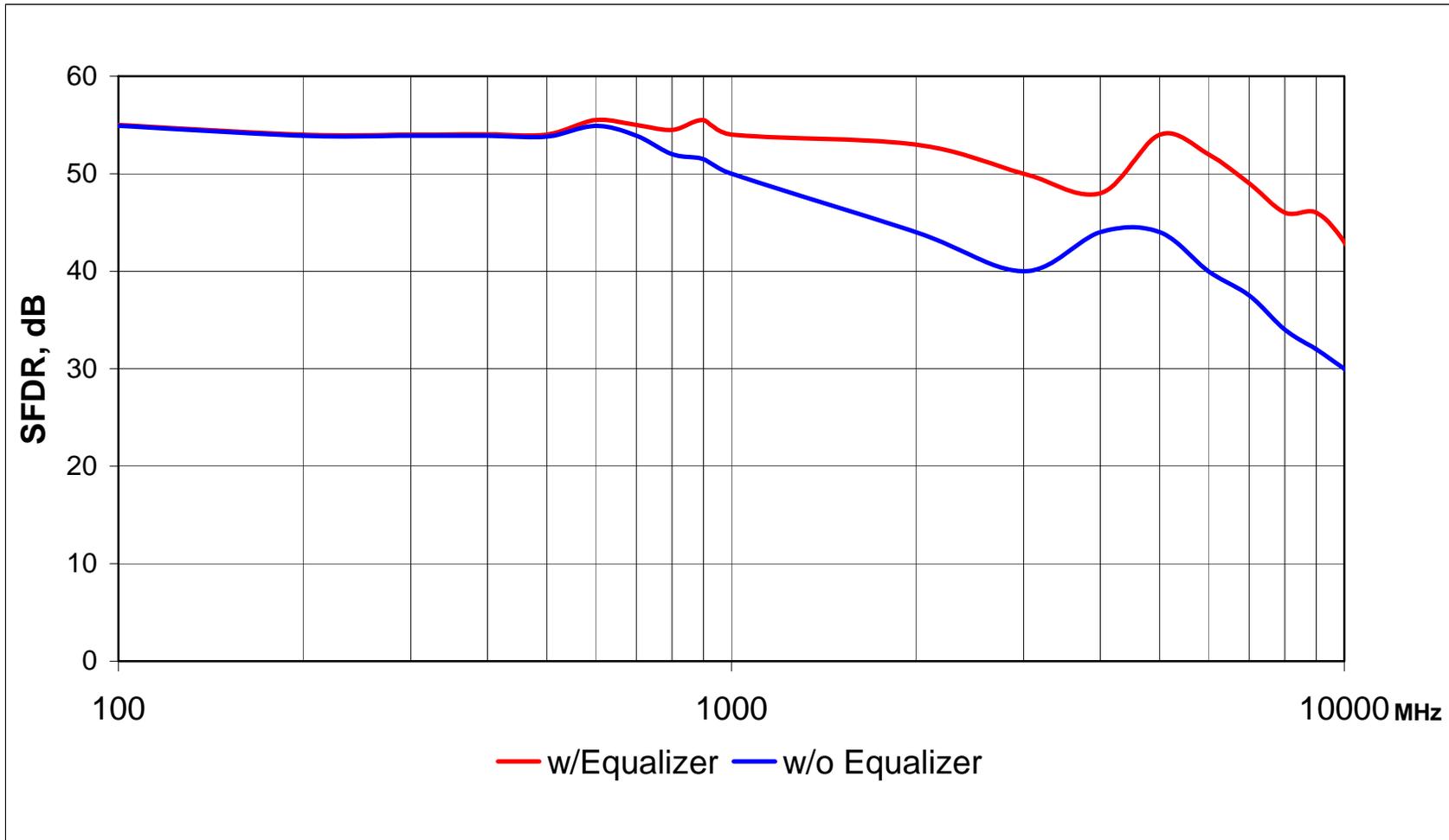
**Figure 4.9 13GHz, 40Gbit/s, 8-Bit Digitizer
FFT of Acquired Signal, 7.132 Ghz, No Equalizer**



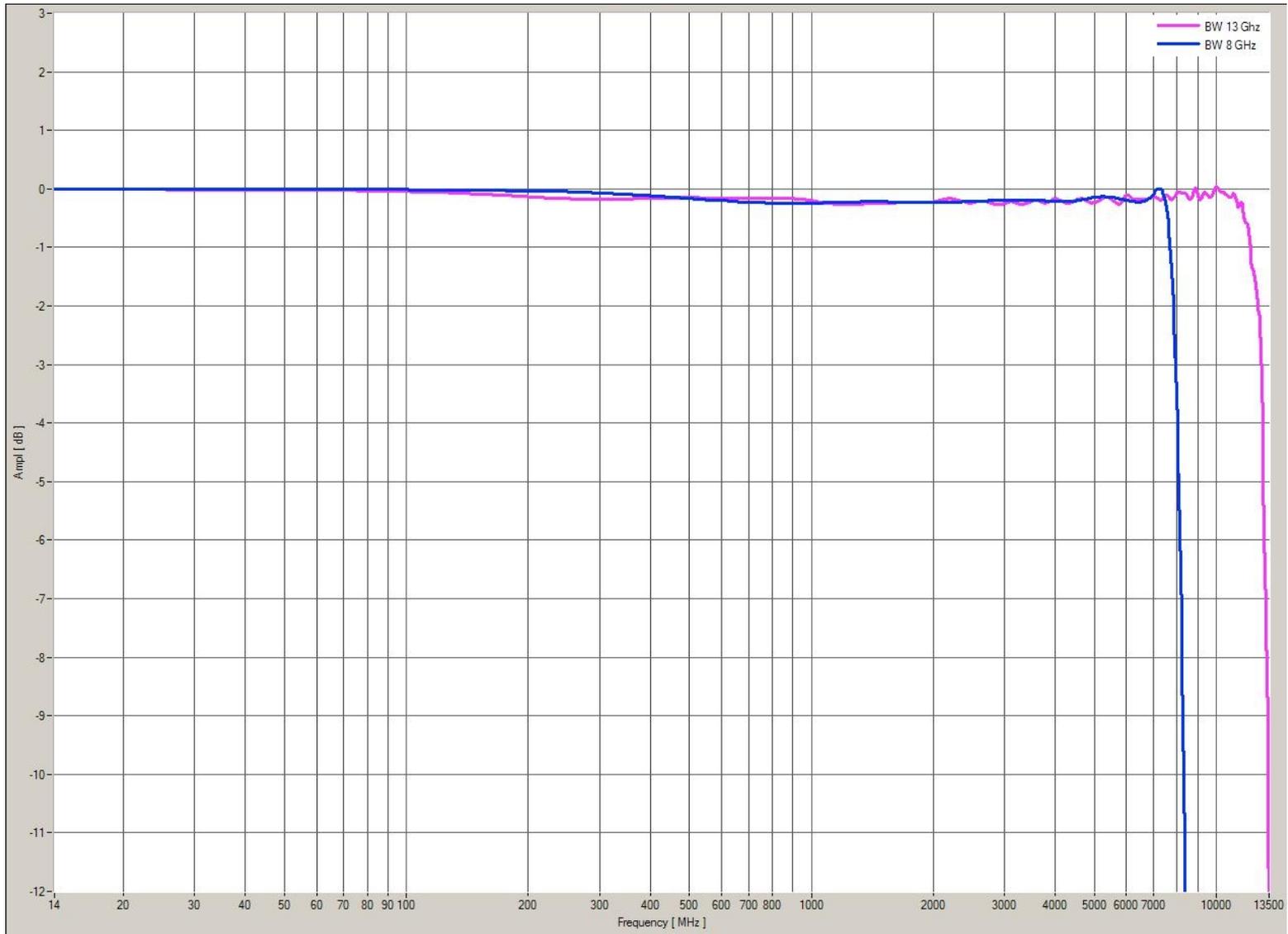
**Figure 4.10 Same as Figure 4.9
With Equalizer and Digital Filter, 13Ghz**



**Figure 4.11 13Ghz, 40Gbit/s, 8-Bit Digitizer
ENOB vs. Frequency**



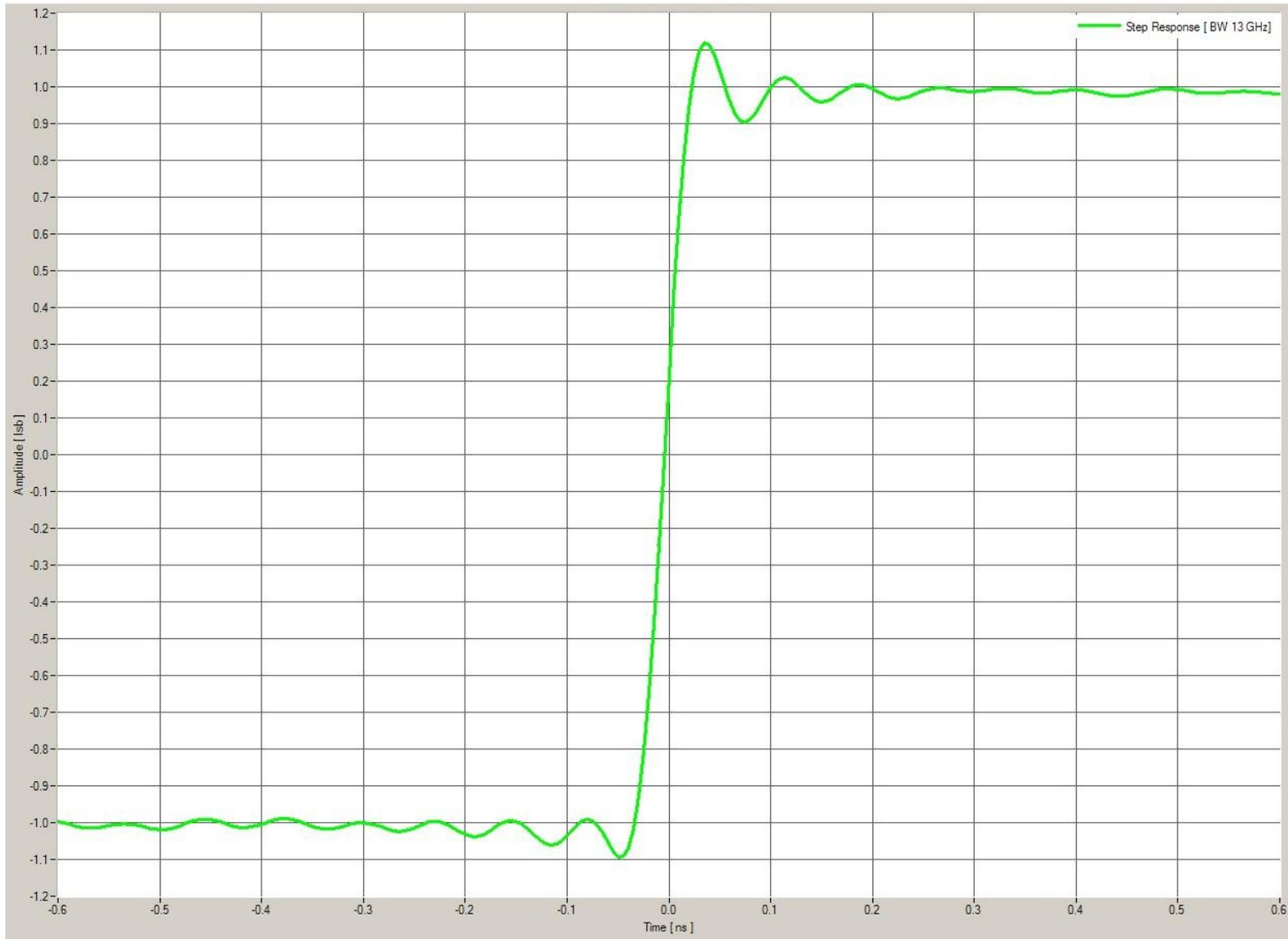
**Figure 4.12 13Ghz, 40Gbit/s, 8-Bit Digitizer
SFDR vs. Frequency**



5.1 13GHz, 40Gs/s and 8GHz, 20Gs/s Digitizers Equalized Frequency Responses



5.2 8GHz, 20Gs/s Digitizer Equalized Step Response



5.3 13GHz, 40Gs/s Digitizer
Equalized Step Response, Overshoot 5.9%, Preshoot 4.7%